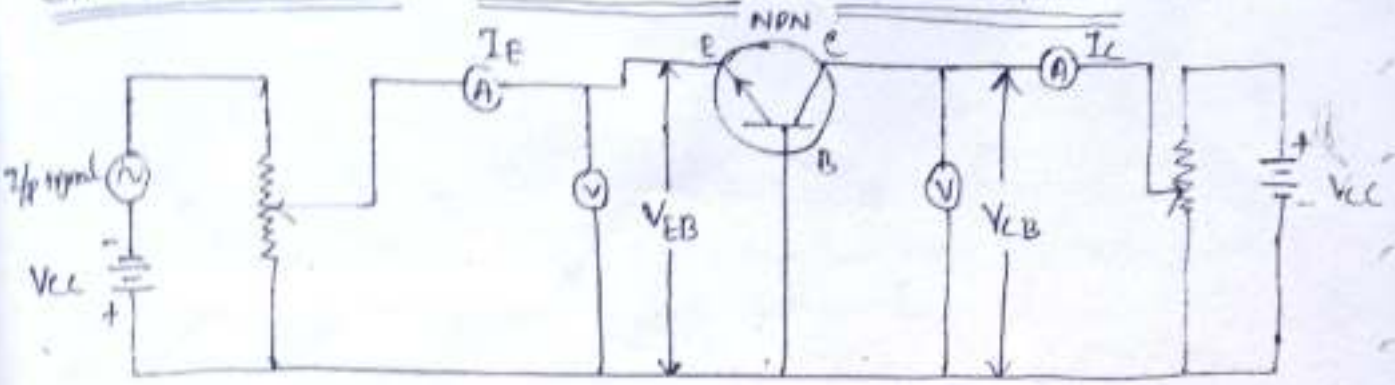
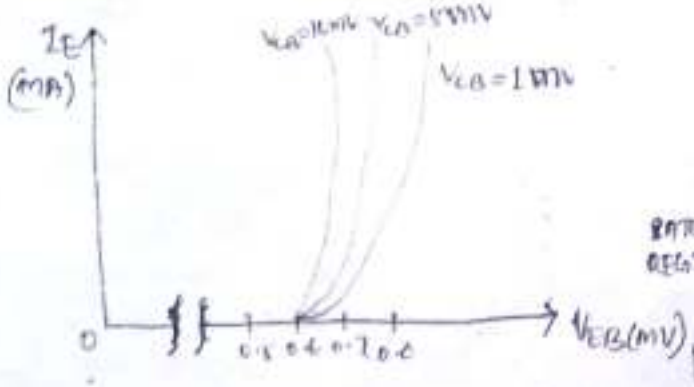
CHARACTERISTICS OF COMMON BASE CONFIGURATION :→



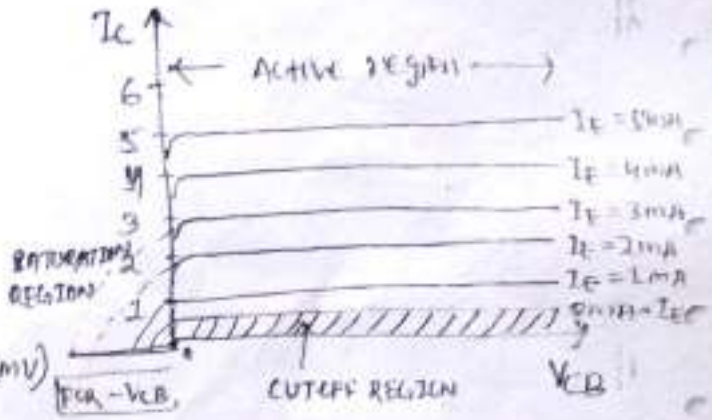
← INPUT CHARACTERISTICS :→

It is the relation between the emitter current (I_E) & emitter to base voltage (V_{EB}).
This characteristics can be drawn by taking collector to base voltage (V_{CB}) constant



← OUTPUT CHARACTERISTICS :—

It is the curve between collector to base voltage V_{CB} & collector current (I_C) at constant input emitter current (I_E).



Input resistance :—

It is the ratio between change in emitter to base voltage (V_{EB}) to the change in emitter current (I_E)

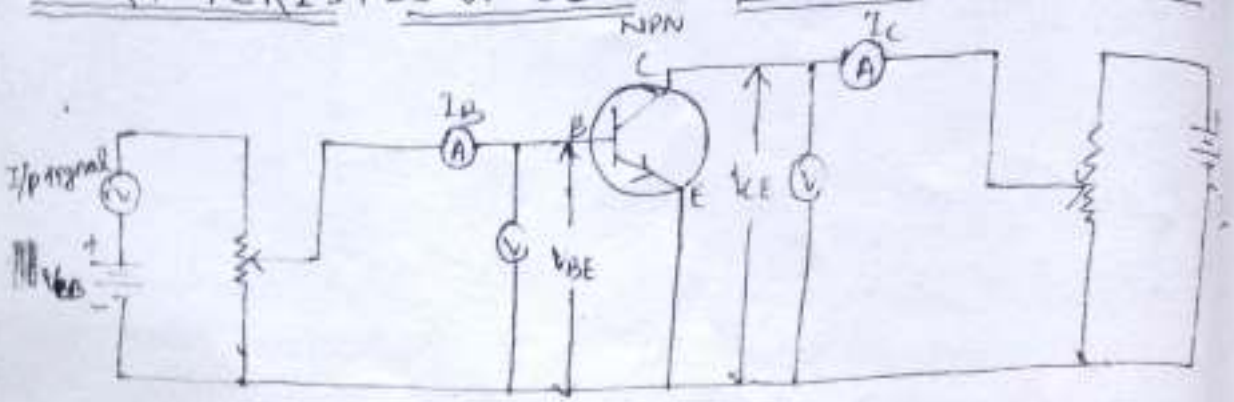
i.e. $$r_i = \frac{\Delta V_{EB}}{\Delta I_E}$$

OUTPUT RESISTANCE :—

It is the ratio between change in collector to base voltage to change in collector current (I_C) at constant I_E.

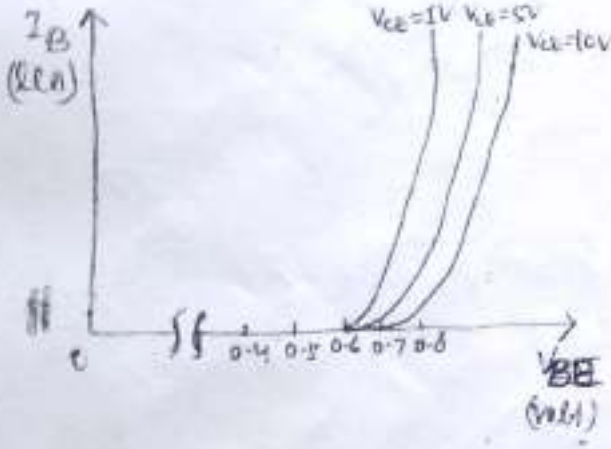
i.e. $$r_o = \frac{\Delta V_{CB}}{\Delta I_C}$$

CHARACTERISTIC OF COMMON EMITTER CONFIGURATION



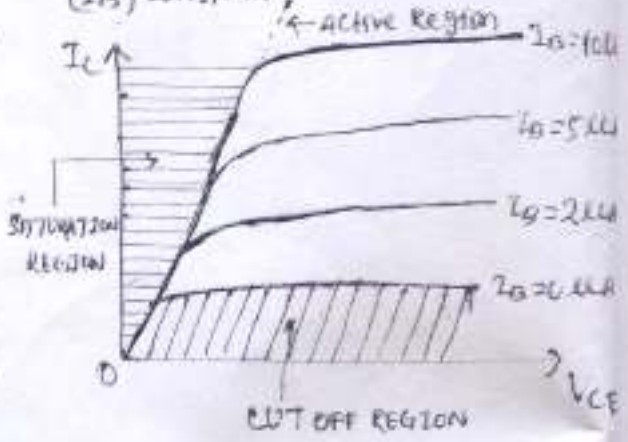
INPUT CHARACTERISTICS:-

The input characteristic can be done by taking V_{BE} & base current I_B at constant V_{CE}



OUTPUT CHARACTERISTIC:-

It is the graph between collector to emitter voltage (V_{CE}) & collector current (I_C) by keeping base current (I_B) constant.



Input resistance:-

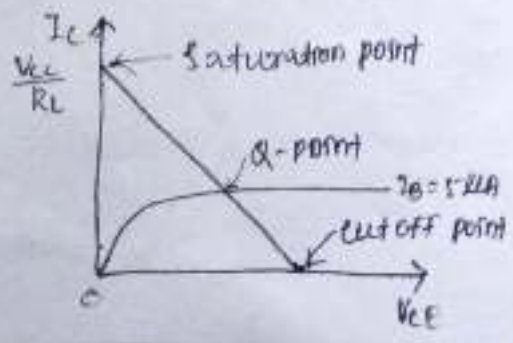
It is the ratio of change in V_{BE} to change in I_B

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B}$$

OUTPUT RESISTANCE:-

It is the ratio of change in V_{CE} to the change in collector current (I_C)

i.e. $$r_o = \frac{\Delta V_{CE}}{\Delta I_C}$$



∵ $I_E = I_B + I_C$

In CC configuration, $I_C = I_E$ so that the characteristic is same with the characteristic of CE configuration.

CHAPTER-15 ← TRANSISTOR CIRCUITS :→

TRANSISTOR BIASING :-

The proper flow of zero signal collector current & maintenance of proper collector to emitter voltage during the passage of signal is known as transistor biasing.

For faithful amplification of a signal three conditions must be satisfied

(i) The base to emitter function should be forward biased
(ii) The base to collector junction should be reverse biased
(iii) There should be proper zero signal collector current.

A transistor is biased either with the help of battery or, associating a ckt with the transistor. The ckt used with the transistor for biasing purpose is called biasing ckt

STABILIZATION :→

The maintainance of the operating point stable is known as stabilization.

⊛ There are different reasons for which the Q-point varies such as

(i) I_C is depend upon temp
(ii) Individual variation
(iii) Thermal runaway

I_C IS DEPEND UPON TEMP :→

(i) The collector leakage current (I_{CEO}) is greatly influence by the temperature. The I_{CEO} doubles for every 10°C of change in temperature.

(ii) When temp increases the β value also increases.

(iii) Variation of V_{BE} is also depends upon temperature.

INDIVIDUAL VARIATION:-

When a transistor is replaced by another transistor of the same type, the value of β & V_{BE} are not exactly same so the operating point varies.

THERMAL RUN AWAY:-

The collector junction has the capacity to exist for changes of temperature 60°C to 100°C for germanium & 150°C to 225°C for silicon.

If the temperature increases beyond this range then the transistor will burn out. This self destruction of an unstabilized transistor is known as thermal runaway.

There are two techniques which are used for stabilization
(1) Stabilization technique
(2) Compensation technique

STABILIZATION TECHNIQUE:-

The technique consists of the use of resistive biasing ckt which maintain the I_c almost constant

COMPENSATION TECHNIQUE:-

In this technique, temperature sensitive devices such as diodes, transistors, thermistors etc. are used to compensate the voltage & current in such away that the operating point is maintain constant.

STABILITY FACTOR:-

Stability factor is defined as the rate of change of collector current (I_c) w.r.t reverse saturation current (leakage current) by keeping β & V_{BE} remain constant.

$$S = \frac{\partial I_c}{\partial I_{CEO}}$$

$$S = \frac{\Delta I_c}{\Delta I_{CEO}}$$

This expression shows that the smaller is the value of S higher is the stability.

EXPRESSION FOR STABILITY FACTOR :→

We know that,

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

Differentiate the above eqn w.r.t I_C considering β constant.

$$\frac{d}{dI_C}(I_C) = \frac{d}{dI_C}\beta I_B + \frac{d}{dI_C}(1+\beta) I_{CBO}$$

$$\Rightarrow 1 = \beta \cdot \frac{dI_B}{dI_C} + (1+\beta) \cdot \frac{d}{dI_C} I_{CBO} \quad \left[\because I_{CBO} \simeq I_{CEO} \text{ AT STABLE 'Q'}\right]$$

$$\Rightarrow 1 = \beta \cdot \frac{dI_B}{dI_C} + (1+\beta) \cdot \frac{1}{S}$$

$$\Rightarrow \frac{1+\beta}{S} = 1 - \beta \cdot \frac{dI_B}{dI_C}$$

$$\Rightarrow \boxed{S = \frac{1+\beta}{1 - \beta \cdot \frac{dI_B}{dI_C}}}$$

If the temperature varies the value of β & V_{BE} also varies so we get two different stability constant. i.e. S_β & S_V.

(A) The stability factor 'S_β' is defined as the rate of change of I_C w.r.t β by keeping I_{CEO} & V_{BE} CONSTANT.

i.e. $$\boxed{S_\beta = \frac{\Delta I_C}{\Delta \beta}}$$

(B) The stability factor 'S_V' is defined as rate of change of I_C w.r.t V_{BE} by keeping I_{CEO} & β constant.

i.e. $$\boxed{S_V = \frac{\Delta I_C}{\Delta V_{BE}}}$$

DIFFERENT METHOD OF TRANSISTORS BIASING:→

There are different methods used for providing biased to transistor are given as follows.

(i) Base resistor method
(ii) Collector to base biased method
(iii) voltage divider biased
(iv) Base biased with collector & emitter feed back.

(A) BASE RESISTOR METHOD:→

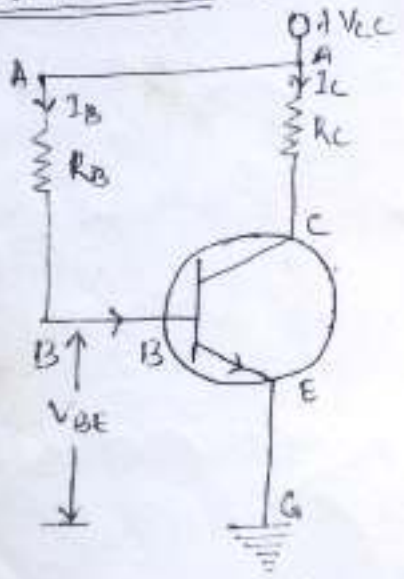


Figure shows an NPN transistor, connected in common emitter configuration with resistor biased. In this method, a high resisti
'R_B' is connected between the terminal of supply & the base of tra

CIRCUIT ANIALYSIS:→

By applying KVL in the loop ABGA, we get

$$V_{cc} = I_B R_B + V_{BE}$$

$$\Rightarrow R_B = \frac{V_{cc} - V_{BE}}{I_B}$$

$$\Rightarrow R_B = \frac{V_{cc} - V_{BE}}{\frac{I_c}{\beta}} \quad \left(\because \beta = \frac{I_c}{I_B}\right)$$

$$\therefore R_B = \frac{\beta\{V_{CC} - V_{BE}\}}{I_C}$$

The value of V_{BE} is very small as compared to V_{CC} so we can write

$$R_B = \frac{\beta(V_{CC})}{I_C}$$

As the value of R_B can be found directly so this method is also called fixed biased method

Stability factor:-

As we know that $S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)}$

In fixed-bias method, I_B is independent of I_C so that

$dI_B/dI_C = 0$

$\therefore$ Stability factor $S = \beta + 1$

Applying KVL in the loop ACGA, we get

$$V_{CC} = I_C R_C + V_{CE}$$

$$\Rightarrow I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

As the stability factor is high & the I_C & V_{CE} are change without depend upon I_B so this method has poor stabilization.

ADVANTAGES:-

① This biasing ckt is very simple as only one resistance R_B is req.

② Biasing conditions can easily be set & the calculations are simple.

DISADVANTAGES:-

① The stability factor is high. Therefore, there are strong chances of thermal runaway.

(B) COLLECTOR TO BASE BIAS :-

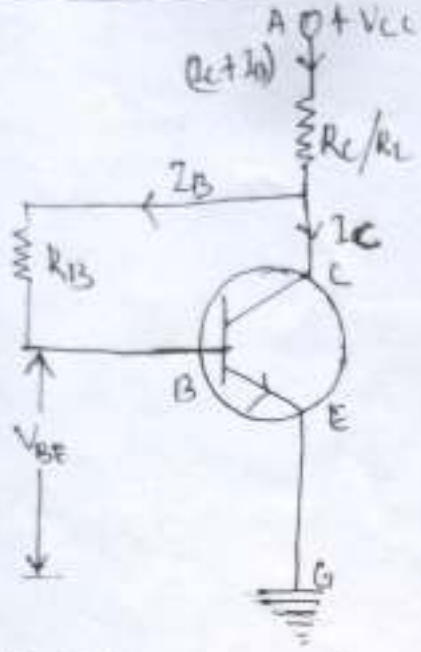


Figure shows the ckt of an NPN transistor connected in common emitter configuration with collector to base biased.

In this method, a resistor is connected between collector & base

CIRCUIT ANALYSIS :-

By applying KVL in ACBGA, we get

$$V_{CC} = (I_C + I_B)R_C + I_B R_B + V_{BE}$$

$$\Rightarrow R_B = \frac{V_{CC} - V_{BE} - (I_C + I_B)R_C}{I_B}$$

$$\Rightarrow \boxed{R_B = \frac{\beta [V_{CC} - V_{BE} - (I_C + I_B)R_C]}{I_C}}$$

We know that,

$$(I_B + I_C)R_C + I_B R_B + V_{BE} = V_{CC}$$

$$\Rightarrow I_B (R_C + R_B) + I_C R_C + V_{BE} = V_{CC}$$

$$\Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B}}$$

Differentiate w.r.t I_B w.r.t I_c, we get

$$\frac{dI_B}{dI_c} = \frac{d}{dI_c}\left[\frac{V_{cc} - V_{BE} - I_c R_c}{R_c + R_B}\right]$$

$$\Rightarrow \frac{dI_B}{dI_c} = \frac{1}{R_c + R_B}\left[\frac{d}{dI_c}\{V_{cc} - V_{BE} - I_c R_c\}\right]$$

$$= \frac{1}{R_c + R_B} \cdot \frac{d}{dI_c}(-I_c R_c)$$

$$= \frac{1}{R_c + R_B} \cdot -R_c = \frac{-R_c}{R_B + R_c} \Rightarrow \boxed{\frac{dI_B}{dI_c} = \frac{-R_c}{R_c + R_B}}$$

Stability factor :-

The stability factor is given by

$$S = \frac{1+\beta}{1-\beta \cdot \frac{dI_B}{dI_c}}$$

$$= \frac{1+\beta}{1-\beta\left\{\frac{-R_c}{R_c + R_B}\right\}}$$

$$= \frac{1+\beta}{1+\beta\left[\frac{R_c}{R_c + R_B}\right]}$$

The stability factor in this method is less as compared to base resistor method so this method is more stabilized.

Q In CB configuration the value of $\alpha = 0.98$ a V.D of 4.9V is obtained across the resistor of 5 KΩ when connected in collector ckt find the base current.

Given data:-

$\alpha = 0.98$ V.D = 4.9V $R_L = 5K\Omega$

$I_c = \frac{V.D}{R_L} = \frac{4.9}{5\times10^3} = 0.98\,mA$

$I_E = \frac{I_c}{\alpha} = \frac{0.98\times10^{-3}}{0.98} = 1mA$

$I_B = I_E - I_c = 1 - 0.98 = 0.02mA$ (Ans).

Q The I_E for a transistor is 3mA & the I_{CBO} is 5μA & $\alpha = 0.98$ calculate the collector & base current.

Given data:-

$I_E = 3mA = 3\times10^{-3}A$

$I_{CBO} = 5\mu A = 5\times10^{-6}A$

$\alpha = 0.98$

$I_c = \alpha I_E = 0.98 \times 3\times10^{-3} = 2.94mA$

$I_B = I_E - I_c = 3 - 2.94 = 0.06mA$

$I_c = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$

$I_B = 0.06mA$ (Ans).

Q. Determine the value of I_E & I_C of a transistor having $\alpha = 0.98$ & CB leakage current $I_{CBO} = 4\mu A$ & the $I_B = 50\mu A$

Given Data:

$\alpha = 0.98$, $I_{CBO} = 4\mu A$, $I_B = 50\mu A$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

$$= 2.65\,mA$$

$$I_E = \frac{I_C}{\alpha} = \frac{2.65}{0.98} = 2.70\,mA \text{ (Amp)}.$$

Q. Determine the biased resistor R_B for fixed biased & collector to base biased & compare the stability factor for both of them.

Given Data:

$V_{CC} = 12V$ $\quad I_B = 0.3\,mA = 0.3\times10^{-3}A$

$R_L = 330\Omega$ $\quad \beta = 100$, $V_{BE} = 6V$

$$I_C = \beta I_B = 100 \times 0.3\times10^{-3} = 0.03A$$

R_B in case of fixed biased

$$= \frac{\beta(V_{CC} - V_{BE})}{I_C} = \frac{100(12-6)}{0.03}$$

$$= 20000\Omega$$

$$= 20K\Omega$$

R_B in case of collector to base biased

$$= \frac{\beta(V_{CC} - V_{BE} - (I_C + I_B)R_L)}{I_C}$$

$$= \frac{100(12-6-(0.03+0.3\times10^{-3})330)}{0.03}$$

$$= -13330\Omega$$

Q. A germanium transistor is to be operated at zero signal I_C equal to 1mA. If the collector supply $V_{CC} = 10V$ what is the value of R_B in base resistor method taking $\beta = 100$.

Given Data:

$I_C = 1mA$, $V_{CC} = 10V$, $\beta = 100$, $V_{BE} =$

$$\therefore R_B = \frac{\beta(V_{CC} - V_{BE})}{I_C}$$

$$= \frac{100(10-0.3)}{1\times10^{-3}} = 970000\,\Omega =$$

If another transistor of same ckt has $\beta = 50$, what will be the new value of zero signal I_C for the same R_B.

$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B}$$

$$= \frac{50(10-0.3)}{970000} = 0.5\,mA$$ (...

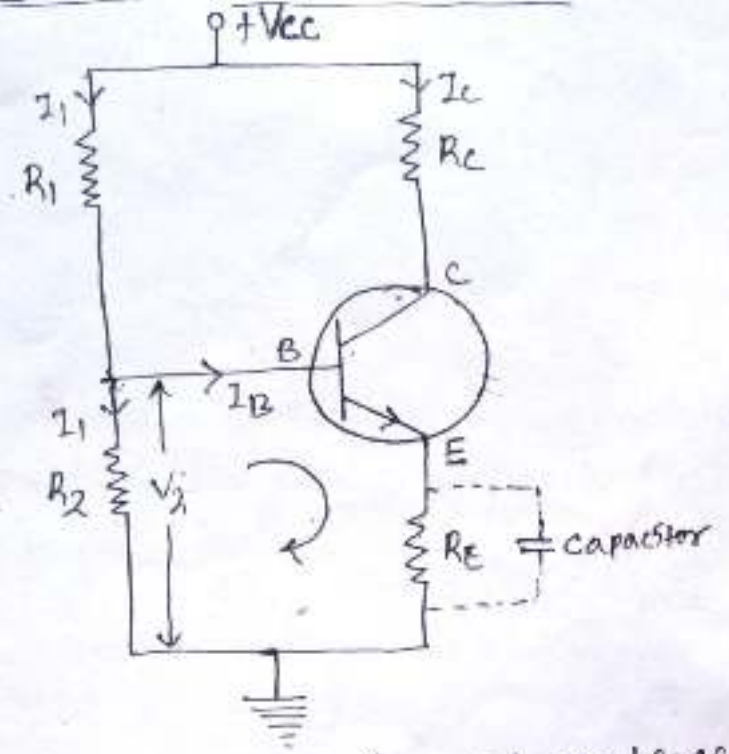
Stability factor of fixed biased is given by $S = 1+\beta = 1+100 = 101$

Stability factor of collector base biased is given by $S = \frac{1+\beta}{1+\beta\left(\frac{R_L}{R_L+R_B}\right)}$

$$= \frac{1+100}{1+100\times\frac{330}{(330-13330)}}$$

$$= -65.65$$

(c) VOLTAGE DIVIDER BIAS METHOD:→



(i) This arrangement is commonly used for biasing of a transistor this is also known as self bias or, emitter bias ckt

(ii) In this method, two resistances R_1 & R_2 are connected across the supply Vcc which provides biasing. The 'R_E' provides stabilization.

(iii) The name voltage divider is derived due to the fact that resistors R_1 & R_2 form a potential divider across Vcc.

(iv) In case of amplifier, to avoid the loss of ac signal gain, a capacitor of large value is connected across 'R_E' resistor which provides a low reactance path for signal.

CIRCUIT ANALYSIS:→

Let,

the current 'I_1' flows across R_1 & also R_2 as the base current is very very small.

The I_1 is given by

$$I_1 = \frac{Vcc}{R_1+R_2}$$

The voltage drop across 'R_2' is given by 'V_2'

$$V_2 = Vcc \times \frac{R_2}{R_1+R_2}$$

Applying KVL to the base circuit, we get

$$V_2 = V_{BE} + I_E R_E$$

$$V_2 = V_{BE} + I_C R_E \quad [\because I_E \simeq I_C]$$

$$\boxed{I_C = \frac{V_2 - V_{BE}}{R_E}}$$

Here, I_C is almost independent of temperature & transistor parameters so this method gives good stabilization.

Applying KVL to the output circuit, we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\Rightarrow V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$\Rightarrow V_{CC} = (R_C + R_E) I_C + V_{CE}$$

$$\Rightarrow V_{CE} = V_{CC} - I_C (R_C + R_E)$$

STABILITY FACTOR :→

Stability factor of voltage divider bias method is given

$$S = \frac{1+\beta}{1+\beta\left[\frac{R_E}{R_B + R_E}\right]}$$

$$= \frac{1+\beta}{1+\beta \cdot \frac{R_E}{R_E\left(\frac{R_B}{R_E}+1\right)}}$$

If R_B value is very very small, it gives better stability

$$\therefore S = (\beta+1) \times \frac{1}{\beta+1} = 1 \Rightarrow \boxed{S = 1}$$

5. In a CE transistor having voltage divider bias have $\beta = 99$, $V_{EE} = 15V$, $V_{CC} = 6V$, $V_{BE} = 0.3V$, $R_C = 2.5k\Omega$, $V_{RE} = 5.5V$ find out the I_C, R_E, I_B.

Sol: We know that,

$$V_{CC} = I_C(R_C + R_E) + V_{CE}$$
$$= I_C R_C + V_{CE} + V_{RE}$$
$$15 = (I_C \times 2.5 \times 10^3) + 6 + 5.5$$
$$\Rightarrow I_C = 1.4mA.$$

$$I_B = \frac{I_C}{\beta} = \frac{1.4 \times 10^{-3}}{99} = 1.414 \times 10^{-5} A$$

$$I_E = I_B + I_C = 1.414 \times 10^{-5} + 1.4 \times 10^{-3}$$
$$= 1.414mA$$

$$R_E = \frac{V_{RE}}{I_E} = \frac{5.5}{1.41 \times 10^{-3}} = 3900\Omega = 3.9k\Omega \text{ (approx)}$$

6. Determine the I_C & V_{CE} for a silicon PNP transistor having $\beta = 50$, $V_{CC} = -20V$, $R_C = 2k\Omega$, $R_E = 0.1k\Omega$ & fixed bias also I_B.

Given data:

$\beta = 50$, $-V_{CC} = -20V$, $R_C = 2k\Omega$

$R_E = 0.1k\Omega$ $V_{BE} = 0.7V$

To find: $I_C = ?$, $V_{CE} = ?$ & $I_B = ?$

$R_1 = 10K\Omega$ $R_2 = 12K\Omega$

$$V_2 = V_{CC} \times \frac{R_2}{R_1 + R_2} = 20 \times \frac{12 \times 10^3}{(10+12)10^3} = 10.91V$$

$$I_C = \frac{V_2 - V_{BE}}{R_E} = \frac{10.91 - 0.7}{0.1 \times 10^3} = 0.102A$$

$$I_B = \frac{I_C}{\beta} = \frac{0.102}{50} = 2.042 \times 10^{-3}$$
$$= 2.04mA \text{ (approx)}.$$

Advantages :-

→ Only one DC supply is necessary.
→ operating point is almost independent of β variation.
→ Operating point stabilized against shift in temperature.
→ less stability factor.

Disadvantages :-

→ More resistors are required as compared to other biasing network.

The ratio of R_1 and R_2 is always 1:10

CHAPTER-6 :- TRANSISTOR AMPLIFIERS AND OSCILLATORS :-

TRANSISTOR AMPLIFIER :-

An amplifier may be defined as a device which increases voltage, current of an input signal with the help of transistor by taking the additional power from external source.

→ When only one transistor with its associated circuit is used for amplifying a weak signal, the amplifier is known as single stage amplifier

→ If there are more than one transistor is used for amplification purpose, it is known as multi-stage amplifier.

CLASSIFICATION OF AMPLIFIERS :-

The amplifiers are classified as follows.

(i) Based on its input :-
They are classified as (a) Small signal amplifier
(b) Large signal amplifier

(ii) Based on its output :-
They are classified as (a) voltage amplifier
(b) power amplifier

(iii) Based on its biasing condition :-
They are classified as (a) class A
(b) class B
(c) class C

* The class A operation is one in which the collector current flows for full cycle of input signal.

(b) The class B amplifiers are those where collector current flows for half cycle of input signal.

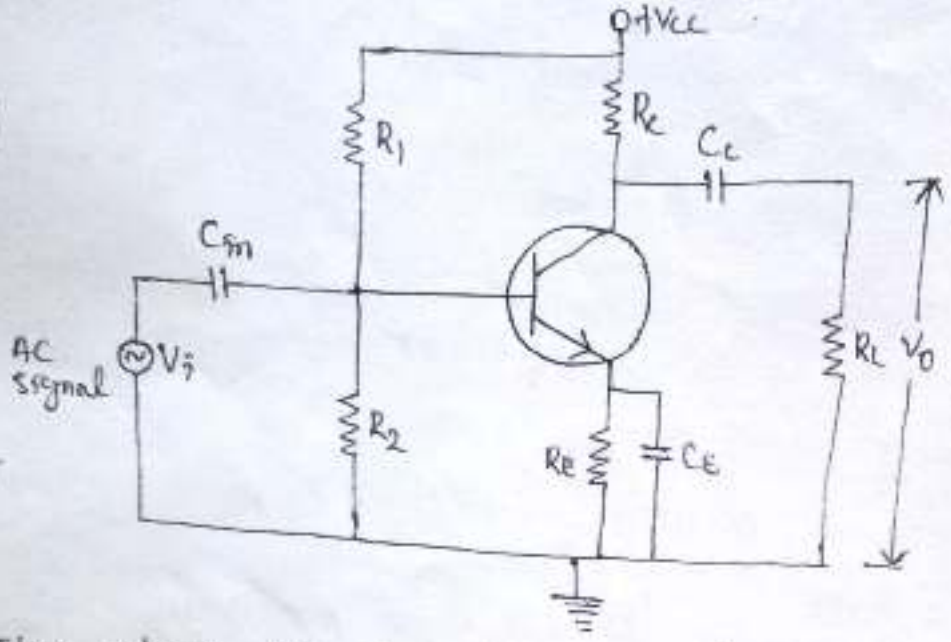
(c) The class C amplifiers are those where collector current flows for less than half cycle of input signal.

(iv) Based on coupling method :-
They are classified as (a) RC coupled amplifiers
(b) Transformer coupled amplifiers.

(V) On the based of transistor configuration :-

They are classified as (a) CB amplifier
(b) CE amplifier
(c) CC amplifier

PRACTICAL CIRCUIT OF TRANSISTOR AMPLIFIER :→



The above fig shows the practical ckt of common emitter transistor amplifier having voltage divider biased. The various ckt elements & their functions are described below.

(i) BIASING CIRCUIT :-

The resistor R_1, R_2 & R_E provides biasing to the transistor for stabilization.

(ii) LOAD (R_L) :-

The resistance 'R_L' connected at the output is known as load resistance. When a no. of stages are used then R_L represents the input resistance of next stage.

(iii) INPUT CAPACITOR (C_{in}) :-

This capacitor couples the signal to the base of a transistor. This is an electrolytic capacitor having value 10μf. This capacitor isolate (separate) the signal shows from R_2.

(iv) COUPLING CAPACITOR (C_c) :-

This capacitor passes ac signal from one side to other side. This is also known as blocking capacitor because it doesn't allow the DC voltage to pass through it. Its value is 10μf

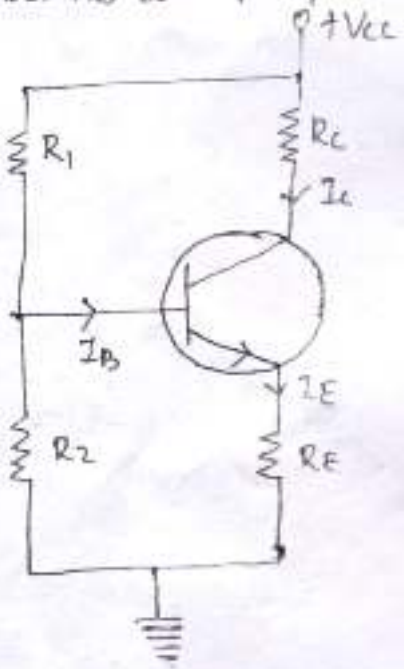
(v) EMITTER BY-PASS CAPACITOR(C_E):-

This is a by-pass capacitor & its value approximately 100μf. This capacitor allows a low reactance path to amplified ac signal. In the absence of this capacitor the voltage developed across R_E will feed back to the input side which reduces output voltage.

LOAD LINE ANALYSIS:-

DC LOAD LINE:-

The DC load line is a line on the output characteristic of a transistor which gives the value of I_C & V_{CE} corresponding to zero signal condition. [AC signal becomes zero & capacitors are opened]



Applying KVL at the output side, we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

put $I_C \simeq I_E$ ($\because I_B$ is very very small)

$$V_{CC} = I_C R_C + I_C R_E + V_{CE}$$

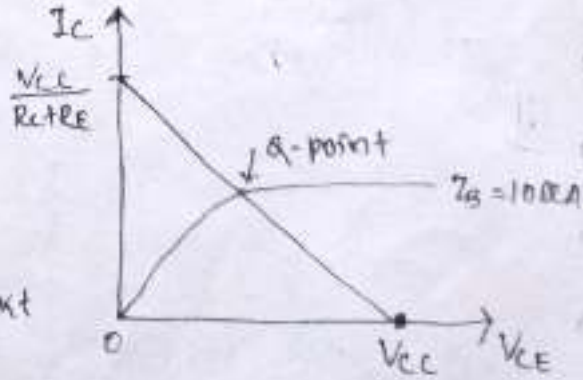
$$V_{CC} = I_C (R_C + R_E) + V_{CE} \quad \text{---} (1)$$

At $I_C = 0$, we get

$$V_{CC} = V_{CE}$$

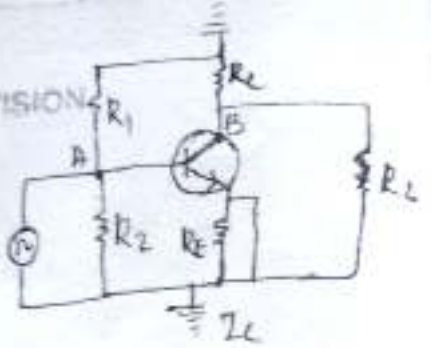
At $V_{CE} = 0$, we get

$$I_C = \frac{V_{CC}}{R_C + R_E}$$



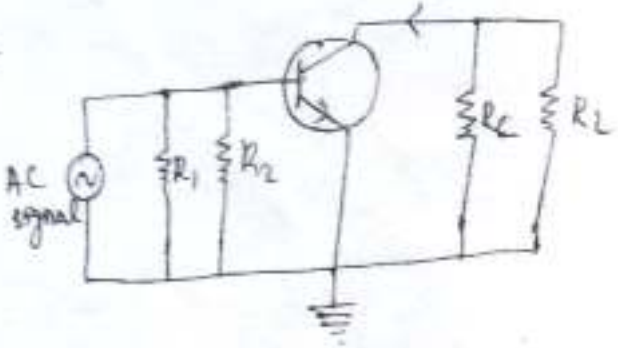
If The value of I_B increases, the Q-point going upward & when I_B decreases the Q-point going downward.

If $I_B = 10\mu A$ is set by the biasing ckt then the intersection point with load line is known as operating point/Q-point.



AC LOAD LINE :-

(i) The AC load line is a line on the output characteristic of a transistor which gives the value of I_C & V_{CE} when signal is applied.



(ii) During AC analysis all the capacitor will be short cut & the DC source reduced to zero.

In AC analysis, the load is given by $R_{ac} = (R_C \parallel R_L) = \frac{R_C R_L}{R_C + R_L}$

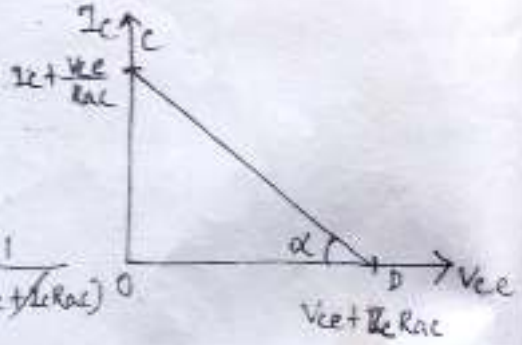
The maximum collector to emitter voltage = $V_{ce} + I_C R_{ac}$

Similarly, The maximum collector current is = $I_C + \frac{V_{ce}}{R_{ac}}$

The slope of AC load line is given by

$$\tan\alpha = \frac{DC}{OD} = \frac{I_C + \frac{V_{ce}}{R_{ac}}}{V_{ce} + I_C R_{ac}}$$

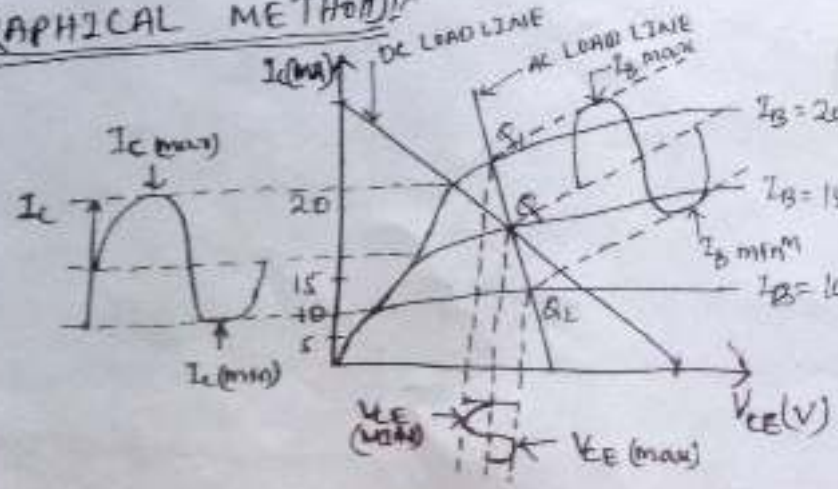
$$= \frac{(I_C R_{ac} + V_{ce})}{R_{ac}} \times \frac{1}{(V_{ce} + I_C R_{ac})}$$



$$\boxed{\tan\alpha = \frac{1}{R_{ac}}}$$

CALCULATION OF GAIN :-

GRAPHICAL METHOD :-

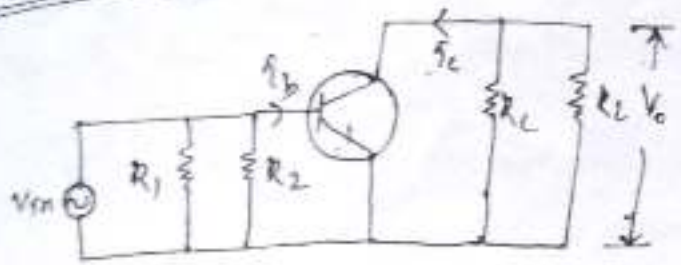


$$\boxed{R_{dc} = R_C + R_E}$$

The voltage gain is given by $A_V = \frac{\Delta V_o}{\Delta V_i} = \frac{V_{CE(max)} - V_{CE(min)}}{V_{i(max)} - V_{i(min)}}$

The current gain is given by $A_i = \frac{\Delta I_o}{\Delta I_i} = \frac{I_{c(max)} - I_{c(min)}}{I_{b(max)} - I_{b(min)}}$

ANALYTICAL METHOD:-



$R_{ac} = R_C \parallel R_L$

The output resistance is given by $R_{ac} = R_C \parallel R_L$

$$R_{ac} = \frac{R_C R_L}{R_C + R_L}$$

The output voltage is given by $V_o = i_c \times R_{ac}$

Suppose the input equivalent resistance is R_{in}, then the input voltage is given by $V_i = I_b R_{in}$

The voltage gain is given by $A_V = \frac{V_o}{V_i} = \frac{i_c \times R_{ac}}{i_b \times R_{in}}$

$$A_V = \beta \times \frac{R_{ac}}{R_{in}}$$

The power gain is given by $A_p = \frac{P_o}{P_i} = \frac{I_c^2 \times R_{ac}}{I_b^2 \times R_{in}}$

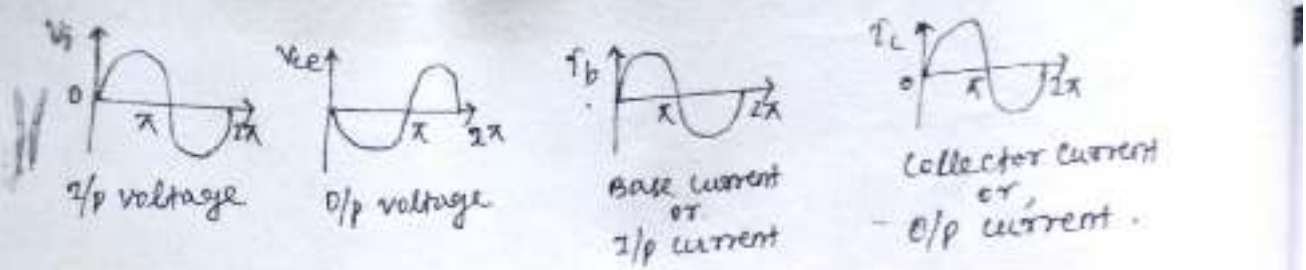
$$A_p = \beta^2 \times \frac{R_{ac}}{R_{in}}$$

The current gain is given by $A_i = \frac{I_o}{I_i} = \frac{I_c}{I_b} = \beta$ $\quad A_i = \beta$

PHASE REVERSAL:→

The phase difference of 180° between the input voltage & output voltage in a common emitter amplifier is known as phase reversal.

Considering the input voltage, i_b, i_c & V_{ce} the wave form can be drawn as follows.



I/p voltage O/p voltage Base current or I/p current Collector current or, - O/p current.

MULTI-STAGE TRANSISTOR AMPLIFIER:→

(i) When the voltage amplification or, power gain of a single stage amplifier is insufficient to meet the requirement then more than one transistor amplifiers are connected in cascade connection it is known as multi-stage amplifier.

(ii) In multi-stage transistor amplifier, the individual stage are connected by the help of coupling circuit.

BLOCK DIAGRAM OF MULTI-STAGE TRANSISTOR AMPLIFIER:

Consider, the individual gain of individual stage amplifier are $A_{V_1}, A_{V_2}, A_{V_3}$ & so on. Then the overall gain of multi stage amplifier is given by

$$A_V = A_{V_1} \times A_{V_2} \times A_{V_3} \times \text{- - - -}$$

There are two purposes for which a coupling device is used such as

(i) To transfer the ac output of one stage to the input of next stage.

(ii) To block the DC to pass from one stage to next stage.

There are different types of coupling devices such as

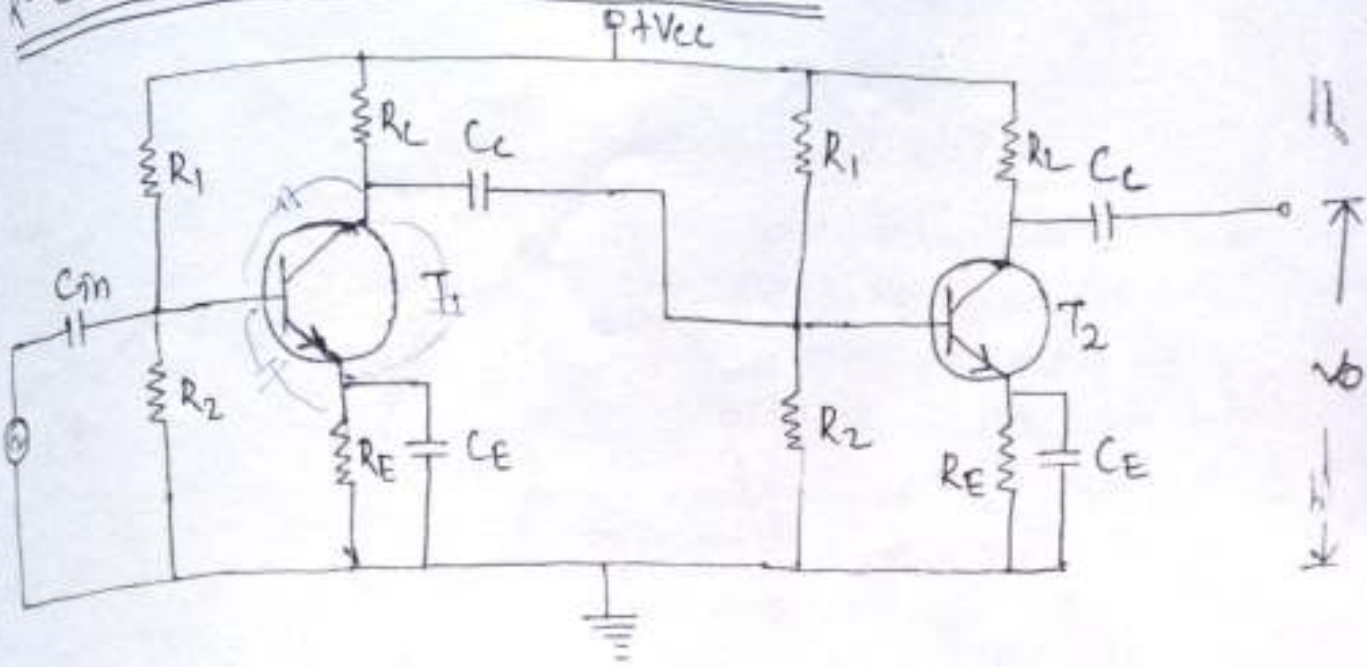
(a) Resistance capacitance (RC) coupling

(b) Transformer coupling

(c) Direct coupling

(d) Impedance coupling.

R-C COUPLED TRANSISTOR AMPLIFIER



CONSTRUCTION WITH OPERATION :-

(i) Fig shows RC coupled transistor amplifier using common emitter configuration. The two transistors (i.e. T_1 & T_2) are identical & connected across a common supply Vcc.
The resistors R_1, R_2 & R_E provides biasing & stabilizing network.
The load resistor 'R_L' is connected across the output of the amplifier.

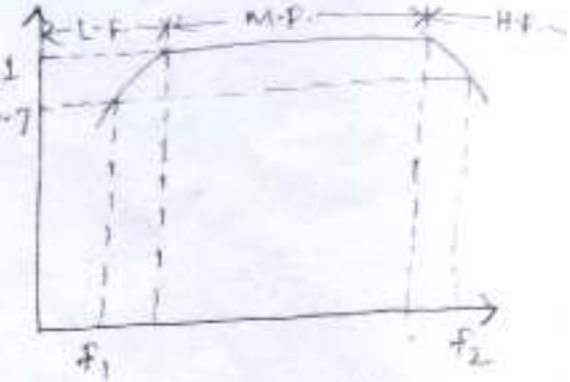
(ii) Here, two stage of amplifier are coupling with a capacitor called as coupling capacitor which provides the output of 1st stage to the input of 2nd stage.

(iii) When AC signal is applied at the input i.e. the base of 1st stage transistor (T_1), it appears across the collector load R_C in amplified form. Through the coupling capacitor (C_C) these amplified signal is fed to the base of next stage transistor (T_2)

(iv) At the load resistor 'R_L' the output signal occurs in amplified form. The phase of output is same as that of input because the phase is reversed twice by two transistor amplifier.

FREQUENCY RESPONSE CURVE:→

(i) In R-C coupled amplifier, the gain decreases at high frequency & low frequency & remain constant for middle range of frequency.



(ii) At low frequency the reactance of coupling capacitor (C_c) is very high so it provides a small part of signal to the next stage so the overall gain decreases.

(iii) At high frequency, there is a formation of capacitance between base-collector, collector-emitter, base-emitter & the two terminal of input supply

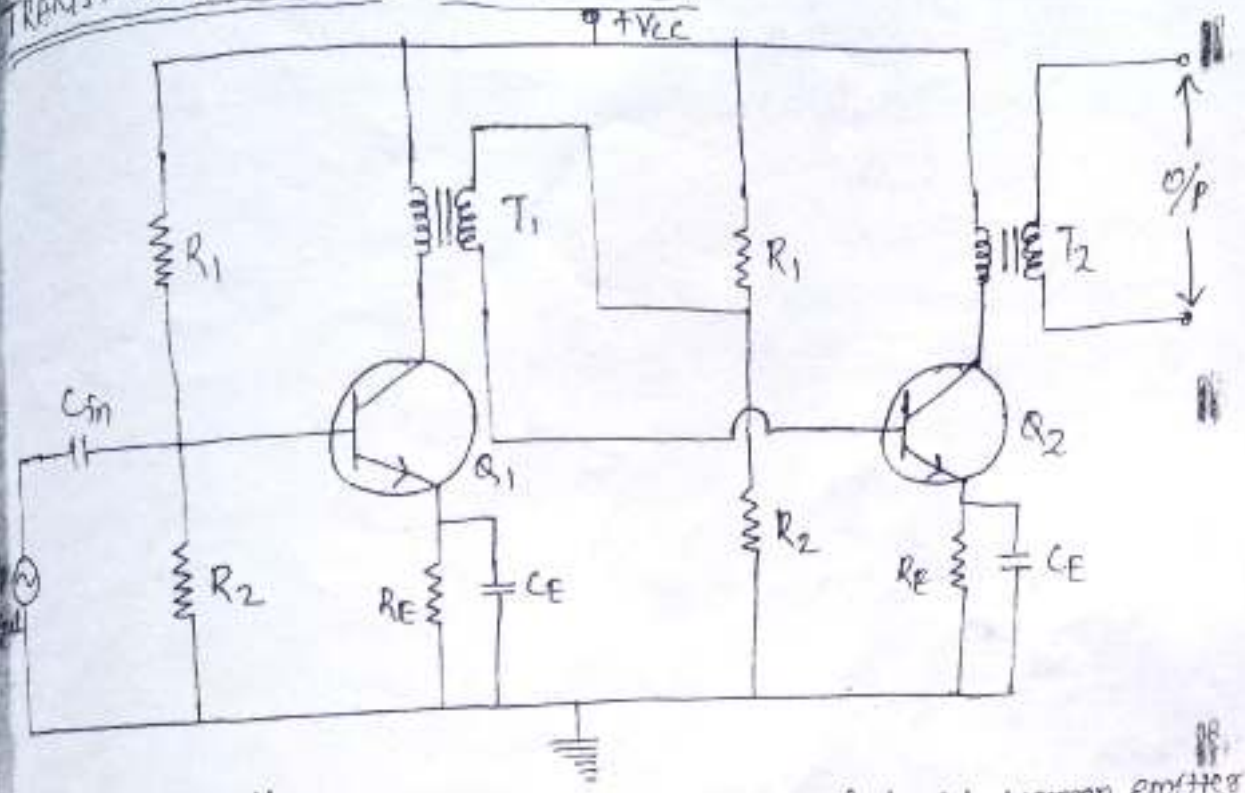
(iv) The capacitive reactance is almost negligible as the frequency is high so it behaves as a short ckt. All the signals are by-passed through this short ckt & does not reach the load so the overall voltage gain decreases.

BANDWIDTH:-

The difference between upper cut-off frequency & lower cut-off frequency is known as bandwidth.

i.e. $\boxed{BW = f_2 - f_1}$

TRANSFORMER COUPLED AMPLIFIER :-



CONSTRUCTION :-

(i) Figure shows two stage transformer coupled with common emitter voltage divider biasing amplifier.

(ii) Here, a coupling transformer (T_1) is used to feed the output of 1st stage amplifier to the input of 2nd stage amplifier. The collector load is replaced by a primary winding of coupling transformer.

(iii) The secondary winding of this coupling transformer is connected to the base of the 2nd stage amplifier. The output is taken from the secondary of transformer at last stage amplifier.

OPERATION :-

(i) When the input is applied to the base of transistor 'Q_1' it is amplified & appears across the primary winding of T_1. By mutual induction this signal is passed to the secondary of 'T_1'.

(ii) Then the output of 'T_1' is fed to the base of transistor 'Q_2' & amplified the signal. Then the signal is appeared at primary of 'T_2' & then this signal can be amplified by next stage amplifier.

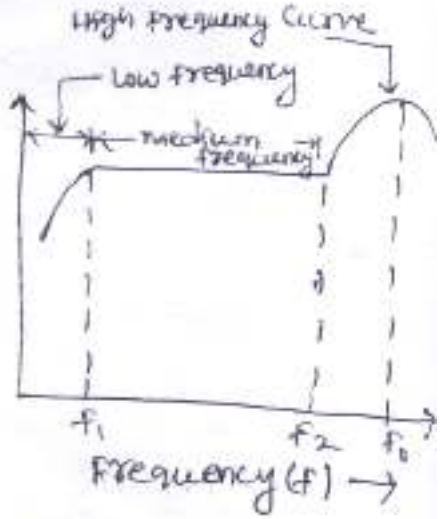
ADVANTAGES :-

1. There is no power loss due to absence of load resistor.
2. It is more efficient
3. It provides excellent power matching
4. It gives high gain.

DISADVANTAGES :-

1. It has poor frequency response
2. It is more costly due to bulky transformer.
3. It introduces a humming sound due to transformer.

FREQUENCY RESPONSE :-



(i) At low frequency of input signal, the amplifier gain is very small & increases upto lower cutoff frequency (f_1)

(ii) After lower cutoff frequency, the gain remain constant for a particular bandwidth i.e. upto higher cutoff frequency 'f_2'.

(iii) After higher cutoff frequency the gain increases upto resonance frequency 'f_0' then decreases.

(iv) For stability of Q-point the gain should be constant which occurs for medium frequency i.e. from f_1 to f_2.

FEEDBACK NETWORK :-

The process of combining of fraction of output back to the input is known as feed back.

There are two types of feed back such as

(a) positive feedback

(b) Negative feedback.

GENERAL THEORY OF FEED BACK :-

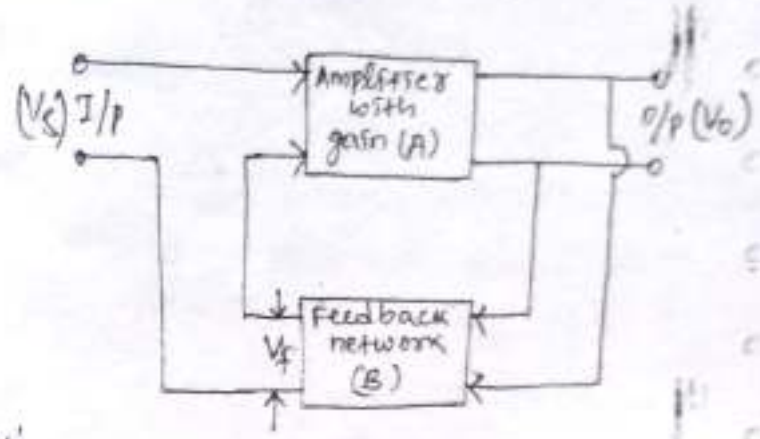


Fig shows the block diagram of general theory of feedback system. This consists of two parts i.e (i) amplifier ckt & (ii) feedback ckt

Normally, the feedback ckt usually consist of resistors

Consider, the Input voltage is 'V_s'.
Gain of the amplifier is 'A'.
output voltage is 'V_o'
Feedback voltage is V_f having gain B.

For +ve feedback, the input of amplifier is given by $V_s + V_f = V_s + BV_o$

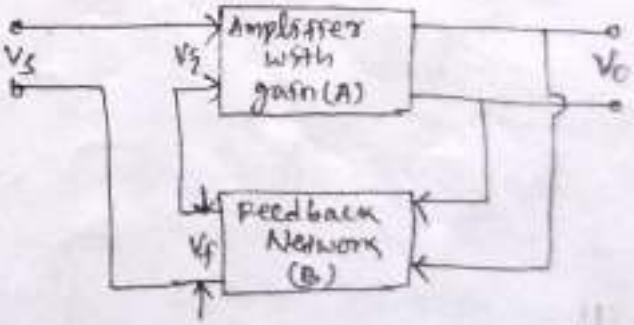
For -ve feedback, the input of amplifier is given by $V_s - V_f = V_s - BV_o$

For +ve feedback, the output voltage is given by $V_o = A[V_s + BV_o]$

For -ve feedback, the output voltage is given by $V_o = A[V_s - BV_o]$

POSITIVE FEEDBACK :-

When the output of feedback network is added with the input supply voltage it is known as positive feedback.



Here, the input voltage of amplifier is given by

$$V_i = V_s + V_f$$
$$= V_s + BV_o$$

We know that

$$V_o = A[V_s + BV_o]$$
$$V_o = AV_s + ABV_o$$
$$\Rightarrow V_o - ABV_o = AV_s$$
$$\Rightarrow V_o(1 - AB) = AV_s$$
$$\Rightarrow \frac{V_o}{V_s} = \frac{A}{1 - AB} \quad \text{---} (1)$$

This eqn indicates the overall gain (A_f) → gain with feedback

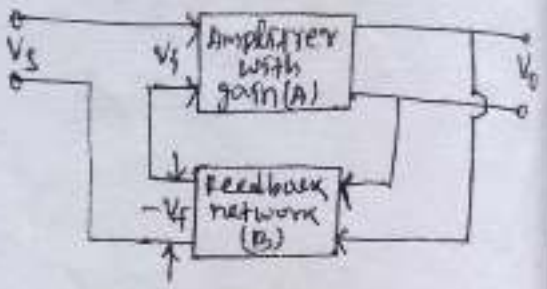
$$\therefore A_f = \frac{A}{1 - AB}$$

NEGATIVE FEEDBACK

When the output of feedback network is difference with the input supply voltage it is known as -ve feedback

Here, the input voltage of amplifier is given by

$$V_i = V_s - V_f$$



we know that $V_o = A[V_s - BV_o]$.

$$V_o = AV_s - ABV_o$$

$$\Rightarrow V_o + ABV_o = AV_s$$

$$\Rightarrow V_o(1+AB) = AV_s$$

$$\Rightarrow \frac{V_o}{V_s} = \frac{A}{1+AB}$$

$$\boxed{A_f = \frac{A}{1+AB}}$$

Q. In a feedback amplifier system, the amplifier produce 100V when 10V is applied to it. The o/p of feedback network is 5V when it takes 50V from the o/p amplifier. Find out the overall gain A_f.

Ans: Given Data:-

$V_o = 100V$ $\quad V_f = 5V$

$V_s = 10V$ $\quad V_o = 50V$

$A = \frac{V_o}{V_s} = \frac{100}{10} = 10$ $\quad B = \frac{V_f}{V_o} = \frac{5}{50} = 0.1$

$\therefore A_f = \frac{10}{1-10\times0.1} = \frac{10}{1-1} = \frac{10}{0} = \infty$

NOTE:-

When $AB = 1$, the overall gain will be ∞ which is a drawback of any system. So we always prefer -ve feedback in the system.

ADVANTAGES OF -VE FEEDBACK:-→

1) It provides stabilization of gain
2) It reduces distortion & noise.
3) It provides high I/p impedance
4) It provides low O/p impedance
5) It increases the bandwidth of a signal of amplifier

TYPES OF Negative Feedback:-

Basically there are two types of -ve feedback such as

(i) Negative voltage feedback
(ii) Negative current feedback.

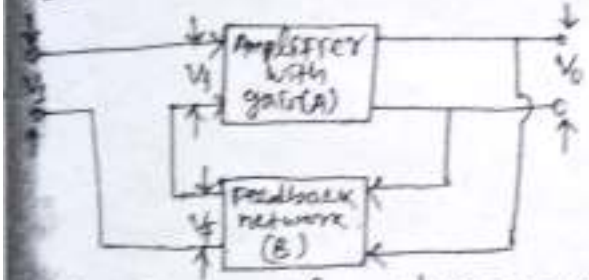
NEGATIVE VOLTAGE FEEDBACK :-

In this method, the voltage feedback to the input of amplifier is proportional to the output voltage.

There are two types of -ve feedback.

(a) voltage series feedback
(b) voltage shunt feedback

voltage series feedback :-



(i) Fig shows a block diagram of voltage series feedback.

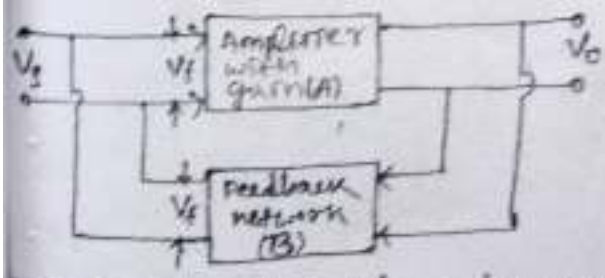
(ii) This is also known as shunt derived series fed feedback.

(iii) Here, some portion of output voltage is applied to the input in series through feedback ckt.

(iv) Here, the output of amplifier is shunted with the input of feedback ckt & the output of feedback ckt is series with the input of amplifier.

(v) It provides low o/p impedance & high I/p impedance.

Voltage shunt feedback :-



(i) Fig shows the block diagram of voltage shunt feedback.

(ii) This is also known as shunt derived shunt fed feedback.

(iii) Here, the output of amplifier is shunted with the input of feedback & the output of feedback is connected in parallel with the input of amplifier.

(iv) Here, both input as well as output impedance are less.

NEGATIVE CURRENT FEEDBACK

In this method, the voltage feedback to the input of amplifier is proportional to the output current.

It is also classified into two types such as

(a) current series feedback
(b) current shunt feedback.

current series feedback :-

(i) Fig shows the block diagram of current series feedback.

(ii) It is also known as series derived series fed feedback.

(iii) Here, the o/p current of amplifier is series with the I/p of feedback network & the o/p of feedback is series with the I/p of amplifier.

(iv) Here, the I/p as well as o/p impedance is high.

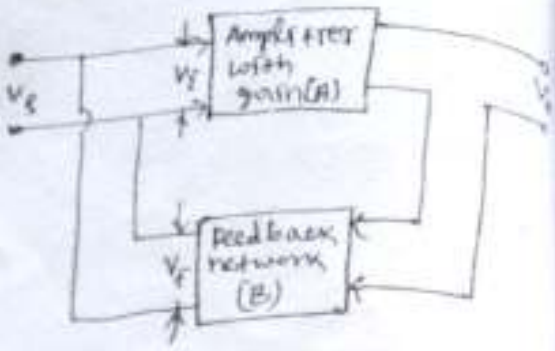
Current shunt feedback :→

(i) Fig shows the block diagram of current shunt feedback.

(ii) It is also known as series derived shunt fed feedback.

(iii) Here, the o/p current of amplifier is series with the I/p of feedback network & the o/p of feed back is shunt with the I/p of amplifier

(iv) Here, the I/p impedance is low & o/p impedance is high.



POWER AMPLIFIER :→

(i) It is an amplifier which amplifies the power level of the signal. It may also defined as a device which converts DC power to AC power & whose action is controlled by input signal.

(ii) Mainly there are two types of power amplifier such as

(a) Audio power amplifier & (b) Radio power amplifier.

(iii) In audio power amplifier, the signal used to amplify have the frequency range from 20Hz to 20KHz. These amplifiers are also known as small signal amplifier.

(iv) In radio power amplifier, the signal is used for amplification having frequency interms of GHz. These amplifiers are also known as large signal amplifier.

TYPES OF POWER AMPLIFIER ON MODE OF OPERATION :→

There are three types of power amplifier such as

(i) class A power amplifier

(ii) class B power amplifier

(iii) class C power amplifier.

DIFFERENCE BETWEEN VOLTAGE AMPLIFIER AND POWER AMPLIFIER

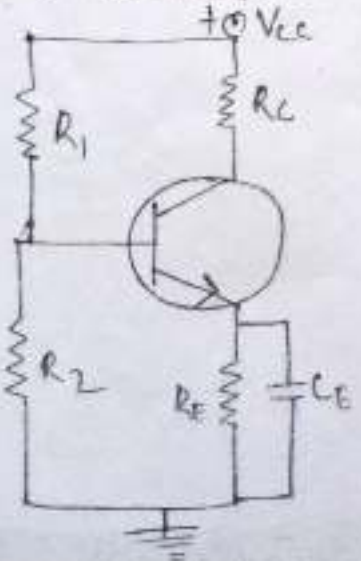
VOLTAGE AMPLIFIER	POWER AMPLIFIER
(i) The function of voltage amplifier is to increase the voltage level of the signal.	(i) The function of power amplifier is to increase the power level of the signal.
(ii) The transistor used in voltage amplifier have high β value.	(ii) The transistor used in power amplifier have low β value.
(iii) In voltage amplifier, the base of transistor is thin.	(iii) In power amplifier, the base of transistor is thick to handle large current.
(iv) The load at the collector is high which provides low collector current.	(iv) The load at the collector is low which provides high collector current.
(v) output impedance is high	(v) output impedance is low.
(vi) Generally R-C coupling is used for multistage amplifier	(vi) Generally transformer & tank ckt coupling is used for multistage amplifier

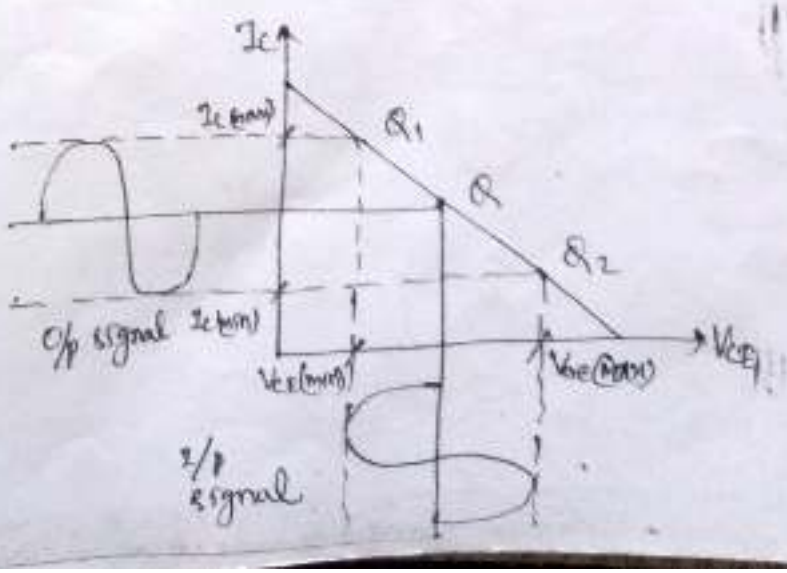
CLASS A AMPLIFIER :→

(i) When the collector current flows at all times during the full cycle of input signal, the power amplifier is known as class A amplifier.

(ii) The operating point (Q) is selected in such away that the transistor operates only for linear region of its load line.

(iii) Here, the output wave form is same as the input wave form.





(i) Fig shows CE configuration voltage divider biased class A amp
The o/p characteristic with the operating point 'Q' is shown in the
(ii) Here, $(I_c)_Q$ & $(V_{CE})_Q$ represents no signal collector current & Collect
to emitter voltage respectively.
(iii) When signal is applied, the 'Q' point shifts between 'Q_1' & 'Q_2'
The collector current varies from $(I_c)_{max}$ to $(I_c)_{min}$ & the Collect
to emitter voltage varies from $(V_{CE})_{max}$ to $(V_{CE})_{min}$.
(iv) The DC power drawn from battery (V_{cc}) is given by

$$P_{in} = V_{cc}(I_c)_Q$$

(v) These power having two parts i.e. (a) power dissipated in the colle
load as heat is given by $P_{RC} = (I_c)_Q^2 \times R_c$

(b) power given to the transistor is $P_{tr} = P_{in} - P_{RC}$

$$\therefore P_{tr} = V_{cc}(I_c)_Q - (I_c)_Q^2 R_c$$

(vi) When signal is applied the power given to transistor having two
parts i.e.

(a) AC power developed across load (R_c) is given by

$$P_{o(ac)} = I^2 R_c = \frac{V^2}{R_c} = \left(\frac{V_m}{\sqrt{2}}\right)^2 \times \frac{1}{R_c} = \frac{V_m^2}{2R_c}$$

where, 'I' is the rms value of AC current.
'V' is the rms value of ac voltage
'V_m' is the max^m value of ac voltage

(b) The power dissipated by transistor in the form of heat is

DIFFERENT TERMS IN POWER AMPLIFIER :→

COLLECTOR EFFICIENCY:-

It is the ratio of AC o/p power to the zero signal power & is expressed as

$$\eta_{collector} = \frac{\text{AC o/p power}}{\text{Avg DC power I/p}}$$

power dissipation capacity:-

The power dissipation capacity is defined as the ability of a power amplifier to dissipate heat developed in it.

Distortion:-

The change of o/p wave shape from the I/p wave shape of the amplifier is known as distortion.

Overall efficiency of class 'A' amplifier:-

It is the ratio of ac power delivered to the load to the total power delivered by DC supply

$$\eta_{overall} = \frac{(P_o)_{ac}}{(P_{in})_{dc}} = \frac{V_{rms} \times I_{rms}}{V_{cc}(I_c)_Q}$$

$$\because V_{rms} \times I_{rms} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}$$

$$= \frac{1}{\sqrt{2}} \left\{ \frac{V_{CE(max)} - V_{CE(min)}}{2} \right\} \times \frac{1}{\sqrt{2}} \left\{ \frac{I_{c(max)} - I_{c(min)}}{2} \right\}$$

$$= \frac{\{(V_{CE})_{max} - (V_{CE})_{min}\} \{(I_c)_{max} - (I_c)_{min}\}}{8}$$

$$\therefore \eta_{overall} = \frac{\{(V_{CE})_{max} - (V_{CE})_{min}\} \{(I_c)_{max} - (I_c)_{min}\}}{8 V_{cc}(I_c)_Q}$$

✱ TRANSFORMER COUPLED CLASS A POWER AMPLIFIER :→

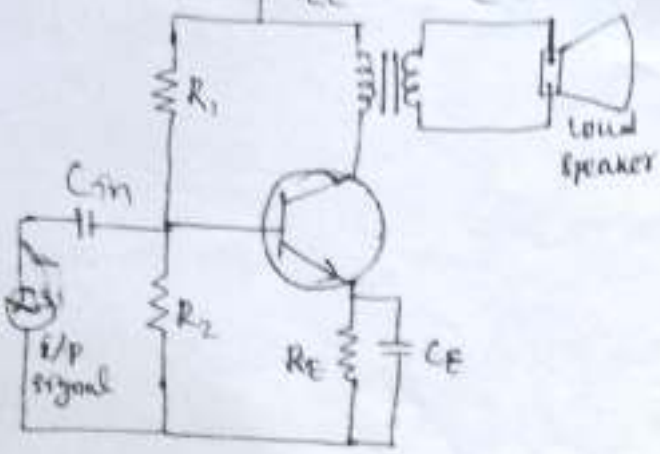
(i) Fig shows the circuit of a transformer coupled class A power amplifier.

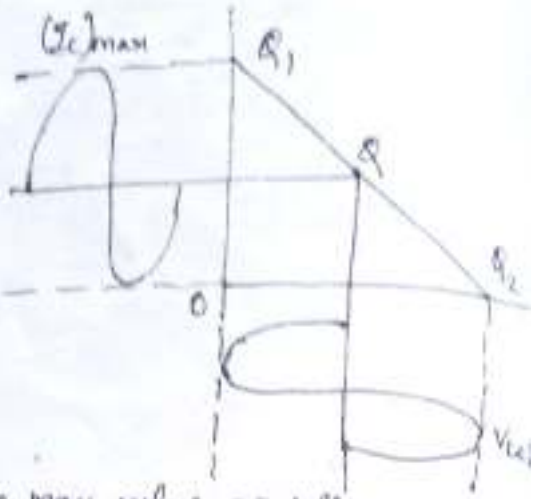
ii) Here, R_1 & R_2 provides biasing & R_E provides the stabilization. The capacitor (C_{in}) blocks any dc from the previous stage. The input signal from pre-amplifier is applied to the input of power amplifier.

iii) Here, a transformer is used as a coupling device having high impedance in primary winding & low impedance in secondary winding.

Primary impedance = (turns ratio)^2 × secondary impedance

1) $Z_1 = \left(\frac{n_1}{n_2}\right)^2 \times Z_2$





(iv) In order to get maximum power the peak value of collector current is considered as the zero signal current of the input signal.

(v) The variation of collector voltage appears across the primary of transformer & a secondary voltage is induced which develops the power in load.

(vi) By considering the power loss in primary winding of transformer is negligible, the i/p power is given by

$$(P_{in})_{dc} = V_{cc} \times (I_c)_Q$$

The o/p power is given by $(P_o)_{ac} = V_{rms} \times I_{rms}$.

$$V_{rms} = \frac{1}{\sqrt{2}} \frac{(V_{ce})_{max} - (V_{ce})_{min}}{2} = \frac{1}{\sqrt{2}} \frac{(V_{ce})_{max} - 0}{2} = \frac{1}{2\sqrt{2}} (V_{ce})_{max}$$

Similarly $I_{rms} = \frac{(I_c)_{max}}{2\sqrt{2}}$

$$\therefore (P_o)_{ac} = \frac{(V_{ce})_{max} \times (I_c)_{max}}{8} = \frac{V_{cc} \times I_c}{8}$$

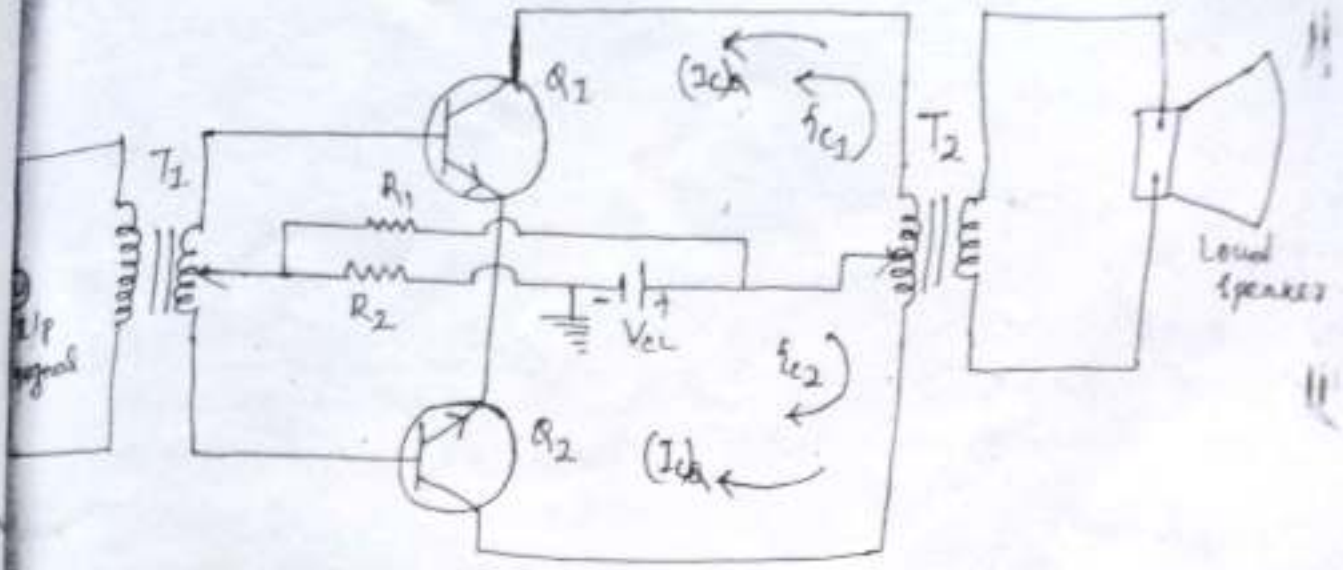
$$\therefore \text{overall efficiency } (\eta_{overall}) = \frac{\frac{V_{cc} \times I_c}{8}}{V_{cc} \times (I_c)_Q} = \frac{1}{8} \cdot \frac{I_c}{(I_c)_Q}$$

$$= 0.125 \frac{I_c}{I_c} = 0.125$$

$$\therefore \eta_{overall} = 12.5\%$$

(vii) In this type of amplifier the efficiency is less than 50%.

CLASS A PUSH-PULL POWER AMPLIFIER :→



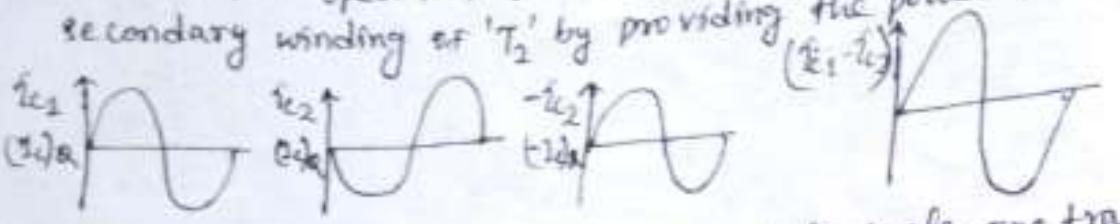
CONSTRUCTION :-

1) Fig shows the ckt diagram of class A push-pull power amplifier
2) Here, two identical transistor 'Q_1' & 'Q_2' are used with emitter terminals are connected to each other.
3) The input signal is applied to the 'Q_1' & 'Q_2' through centre tap transformer 'T_1'
4) The collector of 'Q_1' & 'Q_2' are connected to the primary winding of transformer 'T_2' & the secondary winding of 'T_2' is connected to the loud speaker.
5) V_{cc} is connected between the collector terminal of 'Q_1' & 'Q_2' & ground terminal. R_1 & R_2 provides biasing.

OPERATION :-

1) The zero signal collector current flows in opposite direction through the primary of transformer 'T_2'.
2) When ac +ve half cycle signal is applied to the input of transformer 'T_1', the base of 'Q_1' is more +ve than the base of 'Q_2' so the collector current (i_{c_1}) is more than (i_{c_2}) the resultant current provides the output voltage induced in the secondary winding due to mutual induction. The resultant current is ($i_{c_1} - i_{c_2}$)
3) During -ve half cycle of ac signal the base of transistor 'Q_2' is more +ve than 'Q_1' so the collector current i_{c_2} is more than i_{c_1}, the voltage develop across the load is due to the resultant current ($i_{c_2} - i_{c_1}$).

(iv) The overall operation results an ac voltage induced in the secondary winding of 'T_2' by providing the power to the load.



(v) It is clear that during any given half cycle, one transistor is being driven (pushed) deep into conduction while the other is being like non-conducting (pulled out) hence the name is push-pull amplifier.

ADVANTAGES:→

(i) In class A amplifier, high AC output power is obtained.
(ii) Even harmonics are absent in the output
(iii) The effect of ripple voltage is minimize

DISADVANTAGES:→

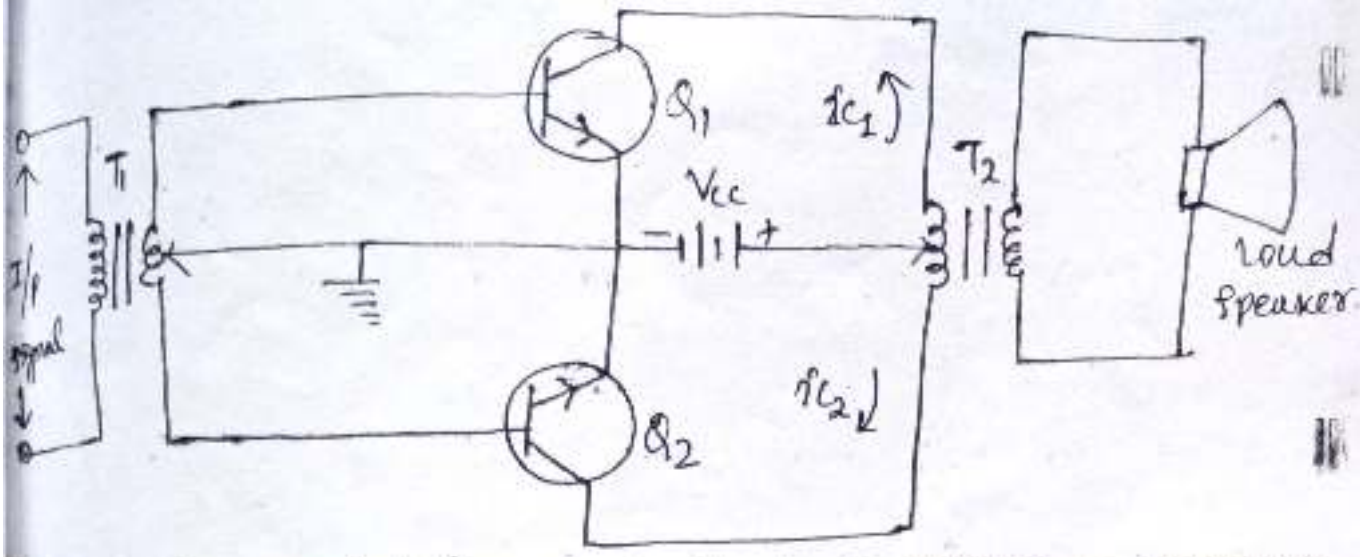
(i) Here two identical transistors are required
(ii) Centre tape transformer is reqd
(iii) The transformer used in this amplifier is bulky & expensive.
(iv) If the characteristics of two transistors are not same, then unequal amplification is obtained at the output.

(*) CLASS-B PUSH-PULL AMPLIFIER :→

(i) When the collector current flows only during the half cycle of input signal, the amplifier is called as class-B amplifier

(ii) In class-B amplifier, the transistor is biased in such a way that at zero signal the collector current is zero so biasing is not required for class-B operation.

(iii) Fig shows class-B push-pull amplifier. The base of two common emitter transistor is connected to the secondary winding of transformer 'T_1' & the input is applied to the primary winding of 'T_1'. The output is taken from the secondary winding of transformer 'T_2'.



(i) In order to get balanced circuit, the emitters of the transistors are connected to the centre tap of secondary of transformer 'T_1' & V_{cc} is applied at the centre tap on primary of transformer 'T_2'

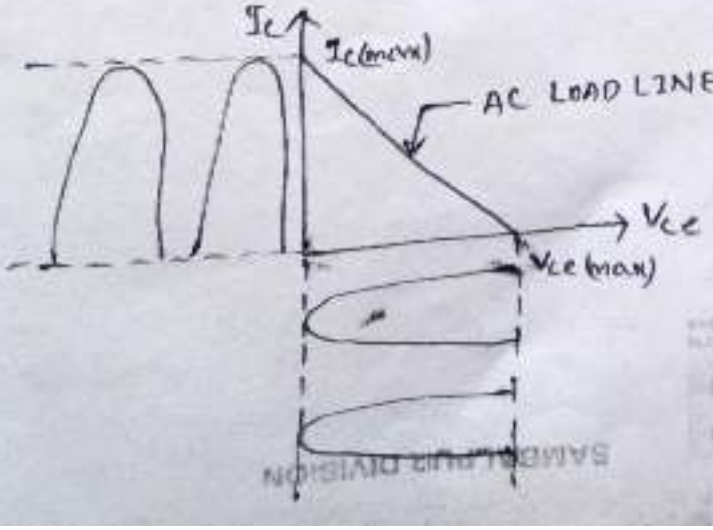
(ii) When no signal is applied both the transistors are in cut off mode. Hence no current is drawn from supply source V_{cc}.

(iii) When input signal is applied, the phase splitter transformer 'T_1' produces two signals which are 180° out of phase with each other during +ve half cycle of input signal.

(iv) During +ve half cycle, the transistor 'Q_1' conducts as the base is +ve & transistor 'Q_2' is in cut off mode. Hence collector current i_{c_1} flows & i_{c_2} is zero.

(v) During -ve half cycle of input signal, the transistor 'Q_2' becomes conducting & 'Q_1' becomes non-conducting. Hence the collector current i_{c_2} flows & i_{c_1} is zero.

(vi) The output transformer 'T_2' joined the two currents producing an almost undistored output wave form.



EFFICIENCY OF CLASS-B AMPLIFIER :→

The average value of DC current is given by $I_{dc} = \frac{I_{c(max)}}{\pi}$

$$P_{in(dc)} = V_{cc} \times I_{dc}$$

$$= \left[V_{cc} \times \frac{I_{c(max)}}{\pi}\right] \times 2$$

The rms value of collector current, $I_{rms} = \frac{I_{c(max)}}{\sqrt{2}}$

Rms value of output voltage $V_{rms} = \frac{V_{cc}}{\sqrt{2}}$

AC output power is given by $P_{o(ac)} = V_{rms} \times I_{rms}$

$$= \frac{V_{cc}}{\sqrt{2}} \times \frac{I_{c(max)}}{\sqrt{2}}$$

$$= \frac{V_{cc} \times I_{c(max)}}{2}$$

$\therefore$ Efficiency $= \frac{P_{o(ac)}}{P_{in(dc)}}$

$$= \frac{\frac{V_{cc} \times I_{c(max)}}{2}}{\left(\frac{V_{cc} \times I_{c(max)}}{\pi}\right) \times 2}$$

$$= \frac{1}{2} \times \frac{\pi}{2} = \frac{\pi}{4} = 0.78$$

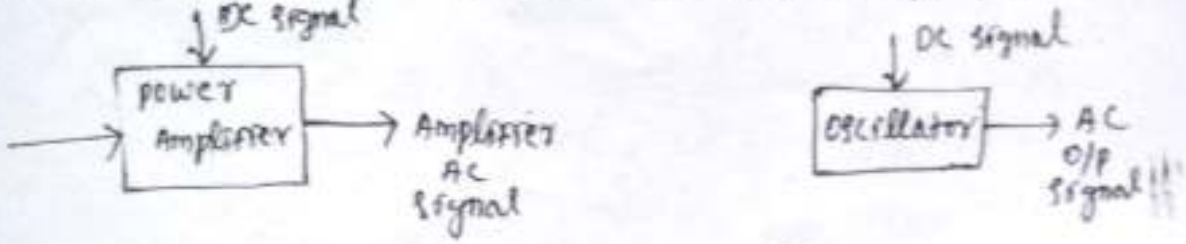
$$= 78\%$$

→ Here the overall efficiency is increased as compared to class A amplifier. As the -ve half cycle is absent the signal distortion is high. When signal increases the transistor dissipates more power.

OSCILLATORS:→

OSCILLATOR:-

(i) Oscillator is a device which can generate an alternating signal. It produces AC power from a DC power without help of input AC signal so oscillator is also called dc to ac converter.



(ii) In oscillator the frequency of the signal is determined by the passive component present in the circuit i.e. inductance & capacitance.

(iii) The oscillator is one type of alternator having some differences such as follows.

ALTERNATOR	OSCILLATOR
(i) It converts mechanical energy to electrical energy	(i) It converts DC energy to AC energy
(ii) It has moving parts so it is called dynamic device.	(ii) It has no moving parts so it is called static device.
(iii) It is large in size	(iii) It is small in size
(iv) It is expensive	(iv) It is cheap
(v) It has more losses	(v) It has less losses
(vi) It produces low frequency signal	(vi) It produces high frequency signal
(vii) More maintanance is required	(vii) Less maintanance is required
(viii) It has complex operation	(viii) It has simple operation.

TYPES OF OSCILLATOR:→

→ Generally the oscillators are of two types according to nature of wave form such as

(a) Sinusoidal oscillator or, harmonic oscillator

(b) Non-sinusoidal oscillator or, Relaxation oscillator

→ According to frequency generated signal oscillators are classified as two types such as

(a) Audio frequency oscillator (20Hz - 20KHz) &

(b) Radio frequency oscillator (more than 20KHz).

AUDIO FREQUENCY OSCILLATOR :→

(1) The oscillator which generates a signal having audio frequency range is called audio frequency oscillator.

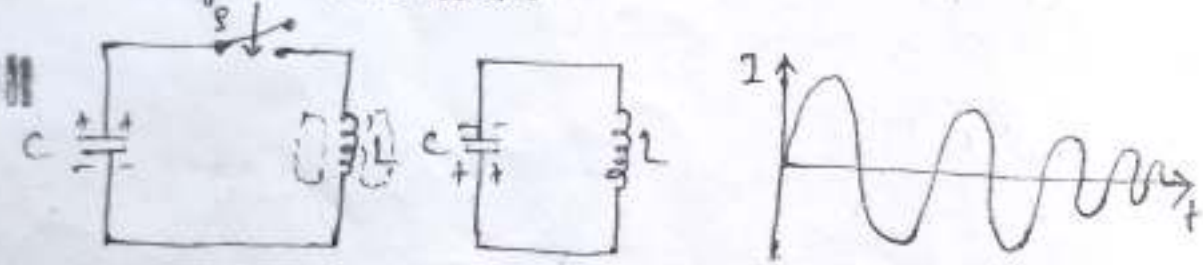
It is classified as different types such as

(a) Tuned ckt oscillator or, L-C feedback oscillator

(b) R-C phase shift oscillator

(c) Negative resistance oscillator

(d) crystal oscillator



The frequency of the signal is given by $f = \frac{1}{2\pi\sqrt{LC}}$

(*) ESSENTIALS OF TRANSISTOR OSCILLATOR :→

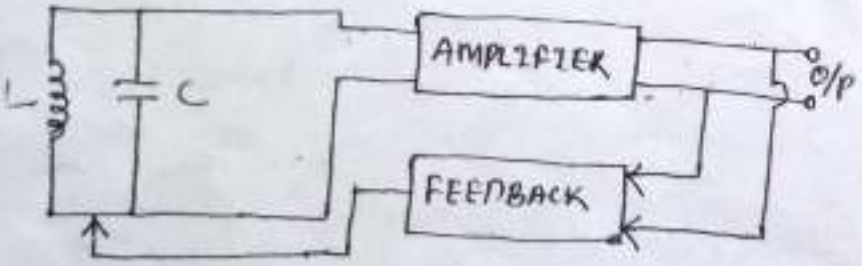


Fig shows the essential components of a feedback LC oscillator which consists of the following circuits.

(1) Tank circuit :—

It consists of an inductance 'L' connected in parallel with a capacitor 'C'. It is also known as frequency determining network.

(ii) Transistor amplifier :-

→ The function of this amplifier is to amplify the oscillations produced by LC circuit.

→ The amplifier receives DC power from the battery & converts it into AC power for supplying to the tank circuit.

→ The transistor used in this amplifier increases the O/p of oscillations.

(iii) Feedback circuit :-

→ The function of feedback circuit is to transfer a part of output energy to LC ckt in proper phase

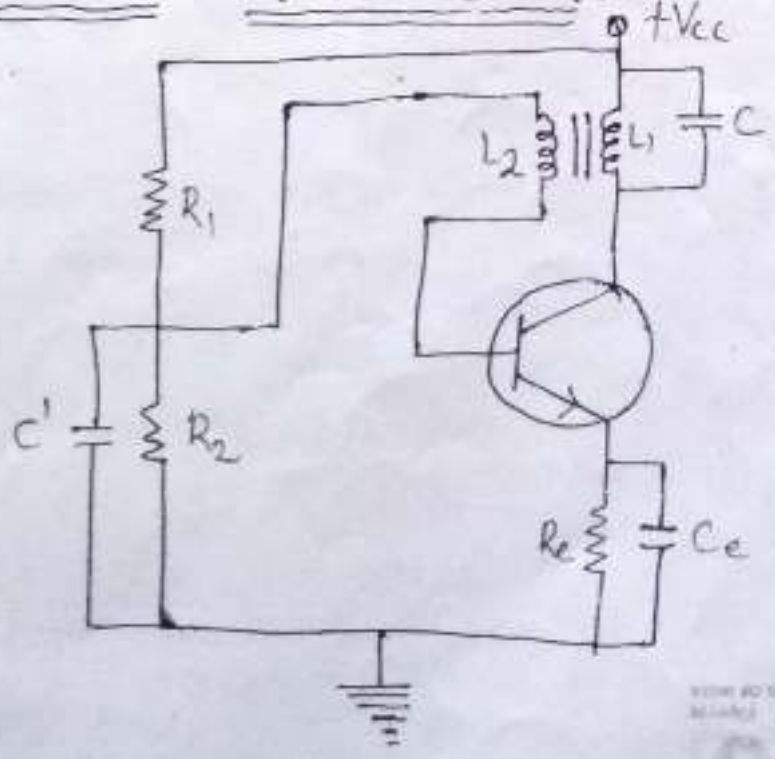
→ When the feedback is +ve, the overall gain of amplifier is given by $A_f = \frac{A}{1-AB}$

If $AB = 1$, then $A_f = \infty$

Here, the gain is ∞ which indicates there is a O/p without giving any input.

→ The condition i.e. $AB = 1$ provides the amplifier works as an oscillator. This condition is known as Bark hausen criterion of oscillation.

TUNNED COLLECTOR OSCILLATOR :→



CIRCUIT ARRANGEMENT :→

(i) The ckt arrangement of a tunned collector oscillator is shown in the fig. Here, the capacitance 'C' is connected with the transformer primary winding inductance 'L_1' which forms a tank circuit. As the tank ckt is connected at the collector terminal, the oscillator is called as collector tunned oscillator.

(ii) The resistors R_1, R_2 & R_e provides biasing & stabilization. The capacitors C_1, C_e & C' are bi-pass capacitors which provides short ckt during AC operation.

(iii) The secondary of transformer is connected to the base of transistor which provides AC feedback voltage.

WORKING PRINCIPLE :-

(i) When the supply is switched 'ON' the collector current starts increasing & charging the capacitor 'C'.
When the capacitor is fully charged, it discharges through inductance 'L_1' & produces oscillations.

(ii) This oscillation induces some voltage in secondary of transformer 'L_2' by mutual induction. These voltage provides the feedback to the amplifier.
The frequency of the oscillation is determined by the value of inductance 'L_1' & capacitance 'C'.

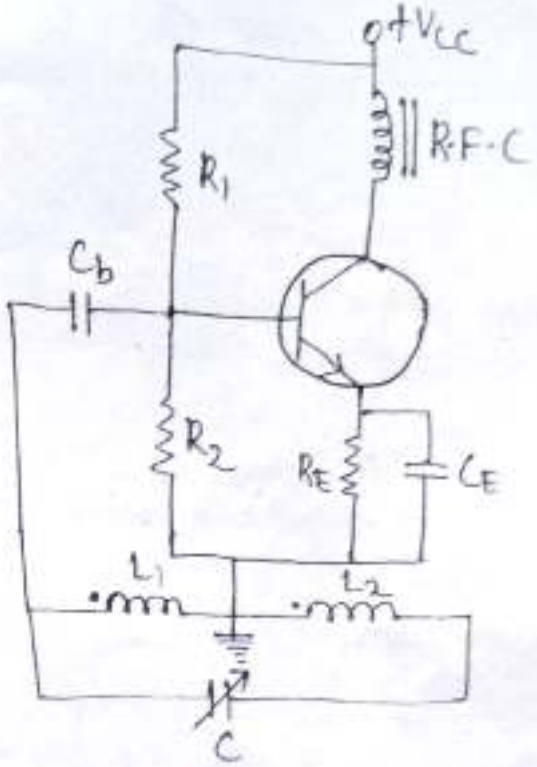
(iii) The feedback voltage provides the variation of base current (I_B) & the collector current is obtained which is equal to β times of input base current (I_B)

(iv) In this way a unknown signal is produced & amplified by the amplifier.

HARTLEY OSCILLATOR :→

CKT ARRANGEMENT :-

(i) Hartley oscillator is commonly used as a local oscillator in radio receiver. The ckt diagram of oscillator is shown in the fig.



(ii) The resistances R_1, R_2 & R_E provides necessary biassing condition & stabilisation. Capacitor C_E & C_b provides bypass path for, ac signal.

(iii) The radio frequency choke (R.F.C) offers very high impedance for high frequency signal i.e. acts like DC short & AC open. Thus it provides DC load for collector & keeps ac current out of DC supply source.

(iv) The frequency determining network consists of inductors L_1 & L_2 across a variable capacitor 'C' as shown in the fig.

(v) The frequency of the signal is determined by $f = \frac{1}{2\pi\sqrt{L_{eq}C}}$

where $L_{eq} = L_1 + L_2 \pm 2M$ ('M' is mutual inductance betn L_1 & L_2)

CKT OPERATION :→

(i) When the collector supply is switched ON the transient current is produced in the tank circuit. This current produces AC voltage across L_2 which provides a feedback between output & Input ckt. This voltage is 180° out of phase with the input supply.

(ii) The common emitter amplifier also produces the voltage which is 180° out of phase with the input of transistor. Thus the total voltage is 360° out of phase with +ve input signal i.e the phase with the input signal.

(iii) The output signal is taken from the winding of L_2 which acts as a auto transformer & provides the feedback to the input which is necessary for oscillator.

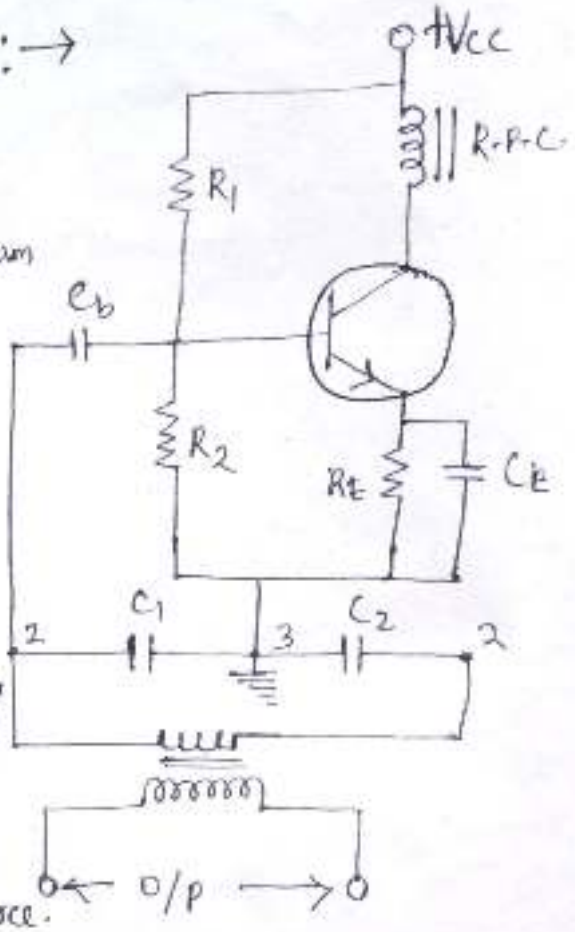
✱ COLPITT OSCILLATOR :→

CKT ARRANGEMENT :→

(i) The fig shows the circuit diagram of colpitt oscillator.

(ii) Here the resistors R_1, R_2 & R_E provides necessary biased condition of the ckt; C_b & C_E provides bi-pass path for AC signal.

(iii) The R.F.C offers very high impedance for the high frequency signal i.e., acts like DC short & AC open. Thus it provides DC load for collector & keeps AC current out of DC supply source.



(iv) The frequency determining network is a parallel resonant circuit which consists of capacitor C_1 & C_2 & inductor 'L'. The junction of C_1 & C_2 is grounded. The voltage developed across C_1 provides feedback voltage required for sustained oscillation.

CKT OPERATION :→

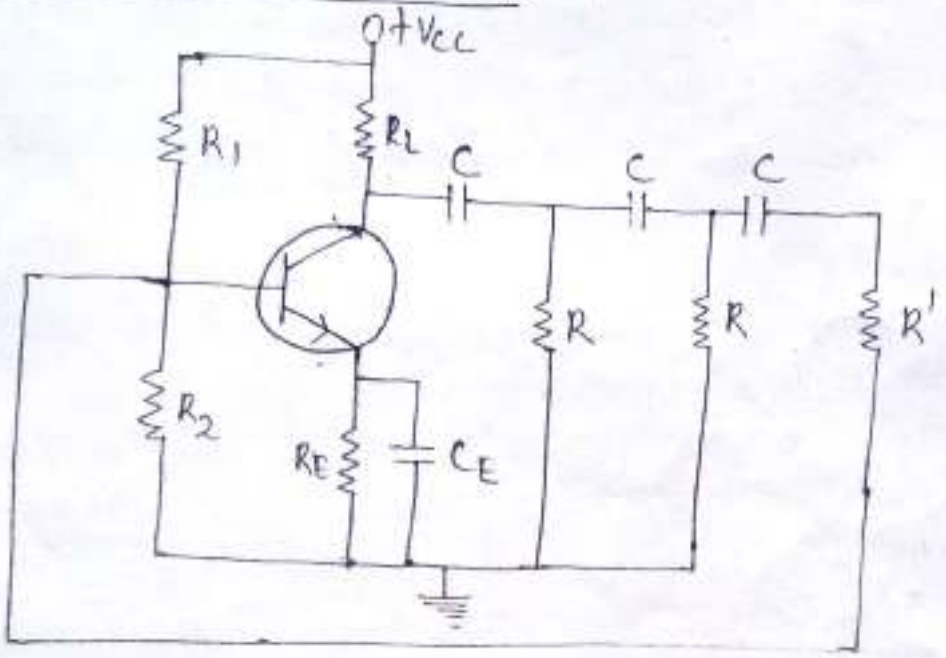
(i) When the collector supply voltage is switch 'ON' the transient current is produced in the tank circuit.

(ii) The oscillation across C_1 are applied to base-emitter junction

(iii) If terminal '1' is +ve potential w.r.t terminal '3' then the terminal '2' will be -ve potential w.r.t terminal '3' as terminal '3' is grounded.

(iv) Therefore terminal 1 & 2 are 180° out of phase. The signal produced by amplifier ckt is also 180° out of phase with the input of amplifier. In this way the oscillator output will be inphase with the input of oscillatory signal.

(x) PHASE SHIFT OSCILLATOR :→



CKT ARRANGEMENT :→

(i) Fig shows the ckt arrangement of phase shift oscillator

(ii) This oscillator is used for producing low frequency signal. Here the signal is produced by R-C network.

(iii) The 180° phase shift in feed back signal can be achieved by taking three arrangements of RC network. The value of R & C may be selected in such a way that for the frequency f' the phase angle is 60°. So using a ladder network of three R-C section, desired 180° phase shift can be achieved.

(iv) Here R_1, R_2, & R_E provides biasing & R_L is the load which controls the collector voltage

(v) The resistance R' is connected between output & input of transistor which provides feedback path.

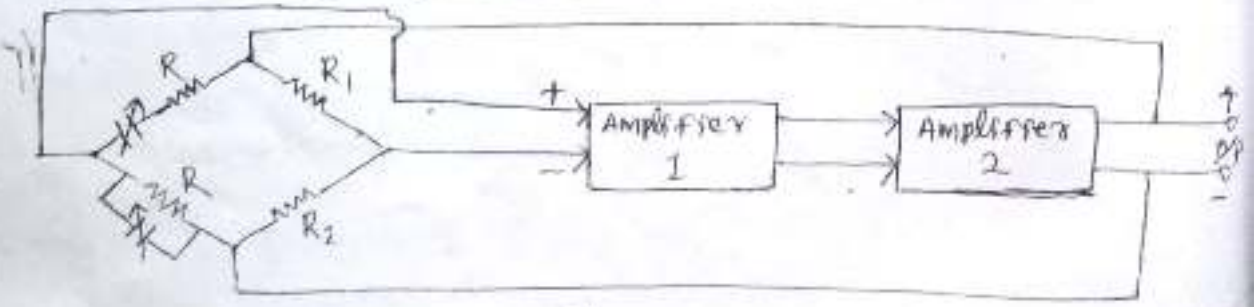
CKT OPERATION:→

(i) Here R-C network produces a phase shift of 180° between input & output voltage. Since common emitter amplifier produces a signal of 180° out of phase thus the total phase shift is 360° or 0° which is in phase with the oscillatory signal.

(ii) This R-C network produces a low frequency signal as compared to LC network & it gives good frequency response.

(iii) The frequency determining ckt produces a signal having frequency $f = \frac{1}{2\pi RC}$.

✳ WIEN BRIDGE OSCILLATOR:→



CIRCUIT ARRANGEMENT:-

(i) Fig shows the ckt diagram of wien bridge oscillator

(ii) This is also known as audio frequency R-C oscillator having the frequency range 10 Hz to 1 MHz

(iii) The oscillator consists of two stage of R-C coupled amplifier & a feed back network.

(iv) The voltage across the parallel combination of R & C is fed to the input of amplifier 1. The net phase shift through the two amplifier is zero.

(v) The wien bridge feedback network provides a signal for a particular frequency so it has good frequency response.

(vi) The frequency of the signal can be varried by varying the two variable capacitor simultaneously

CIRCUIT OPERATION :→

(i) Here, R-C network produces a phase shift of 180° between Input & output voltage since common emitter amplifier produces a signal of 180° out of phase, thus the total phase shift is 360° or, 0° which is inphase with the oscillatory signal.

(ii) This R-C network produces a low frequency signal as compared to L-C network & it gives good frequency response. The frequency determining ckt produces a signal having frequency $f = \frac{1}{2\pi RC}$

ADVANTAGES :-

(i) This gives good frequency stability

(ii) Overall gain is high becoz of two amplifiers

(iii) It produces good sinewave output

DISADVANTAGES :-

(i) It requires two transistors & large no of components

(ii) It can't generate high frequency

✱ H-PARAMETERS OF TRANSISTORS :→

The equation of H-parameter is given by

$$V_1 = h_{11} I_1 + h_{12} V_2$$

$$I_2 = h_{21} I_1 + h_{22} V_2$$

Where,

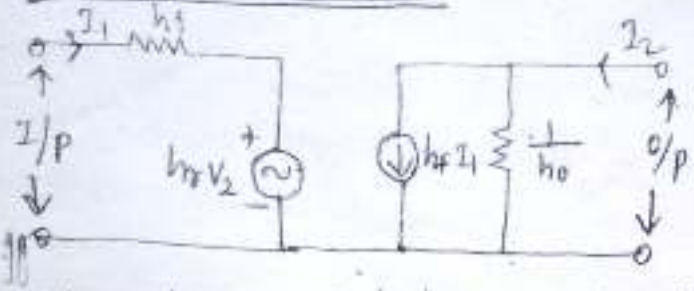
$h_{11} = h_i = \frac{V_1}{I_1}$ [Input impedance]

$h_{12} = h_r = \frac{V_1}{V_2}$ [Reverse voltage gain]

$h_{21} = h_f = \frac{I_2}{I_1}$ [Forward current gain]

$h_{22} = h_o = \frac{I_2}{V_2}$ [output admittance]

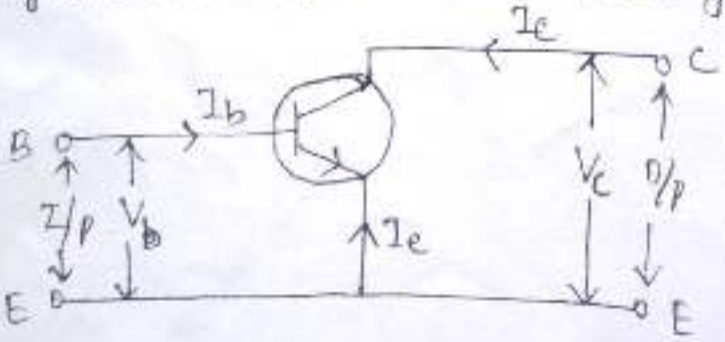
Equivalent circuit :-



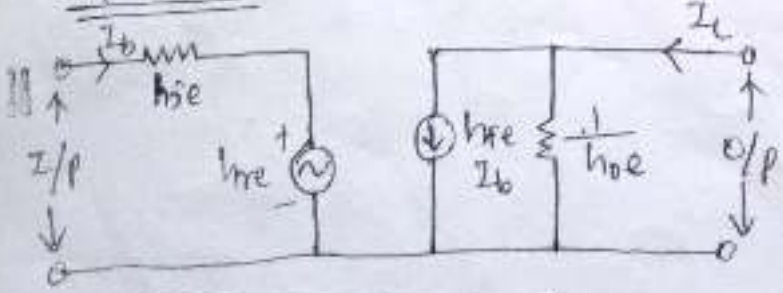
The different 'h' parameter of transistor with different configuration are given below.

h-parameter	CE	CB	CC
$h_{11} = h_i$	h_{ie}	h_{ib}	h_{ic}
$h_{12} = h_r$	h_{re}	h_{rb}	h_{rc}
$h_{21} = h_f$	h_{fe}	h_{fb}	h_{fc}
$h_{22} = h_o$	h_{oe}	h_{ob}	h_{oc}

The hybrid model of CE transistor is given below.



EQ. CKT :-



$$V_b = h_{ie} I_b + h_{re} V_c$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

Dt: 11/10/15

TRANSISTOR AMPLIFIER & OSCILLATORS:-

CHAPTER-06

SIMPLIFIED CE HYBRID MODEL:-

Consider, the resistance $\frac{1}{h_{oe}}$ is very high w.r.t load resistance R_L. So the collector current is given by $I_c = h_{fe} I_B$

The output voltage across the load is given by $V_c = I_c R_L$

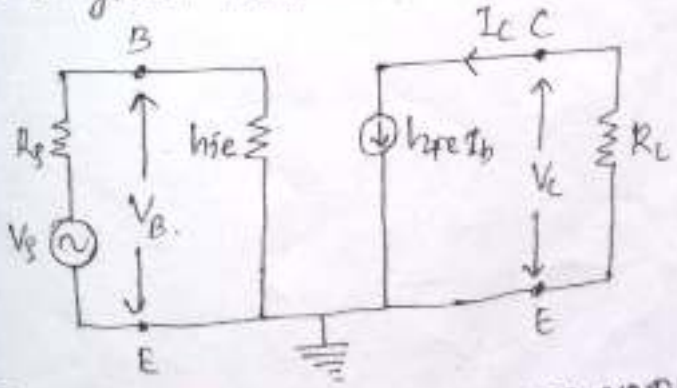
$$V_c = h_{fe} I_b R_L$$

Now,

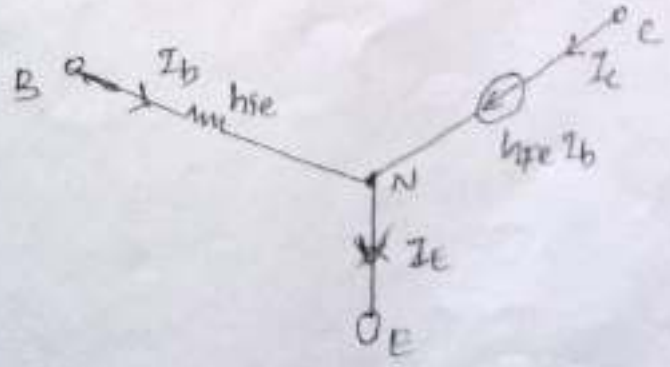
$$h_{re} V_c = h_{re} h_{fe} I_b R_L$$

Since,

$h_{re} \cdot h_{fe} \simeq 0.01$, so these voltage is neglected as compared with the voltage drop across 'h_{ie}' provided that R_L is not too large. Thus the two parameters h_{re} & h_{oe} are neglected to approximate CE hybrid model. So the simplified approximate hybrid model CE is given below.



⊛ GENERALISED APPROXIMATE MODEL:→



(i) Fig shows the generalised approximate model. This can be used for any configuration by grounding the appropriate terminal.

(ii) The signal is always applied between input terminal & ground while the impedance is connected between output terminal & ground.

✱ FIELD EFFECT TRANSISTOR :→

CHAPTER-07

FET:→

The field effect transistor is a three terminal unipolar semi-conductor device in which the current is controlled by the electric field.

It is of two types i.e.

(a) JFET → Junction field effect transistor

(b) MOSFET → Metal oxide semiconductor field effect transistor

✱ COMPARISON BETWEEN BJT & FET:→

BJT	FET
(i) It is a bi-polar device	(i) It is a uni-polar device.
(ii) It is a current control device.	(ii) It is a voltage control device.
(iii) The three terminals are emitter, base & collector.	(iii) The three terminals are drain, gate, source
(iv) It has high noise level	(iv) It has low noise level
(v) It has low input impedance	(v) It has high input impedance
(vi) The gain is characterised by voltage gain.	(vi) The overall gain is characterised by transconductance.
(vii) It has less thermal stability.	(viii) It has better thermal stability

✱ JFET :→

SOURCE:-

The source (S) is a terminal through which the majority charge carrier enters the bar.

DRAIN:-

The drain is a terminal through which the majority charge carrier leave the bar.

GATE:-

These are two internally connected heavily doped impurity regions which forms two PN junctions.

CHANNEL:-

The space between two gates through which the majority carriers pass.

CONSTRUCTION:-

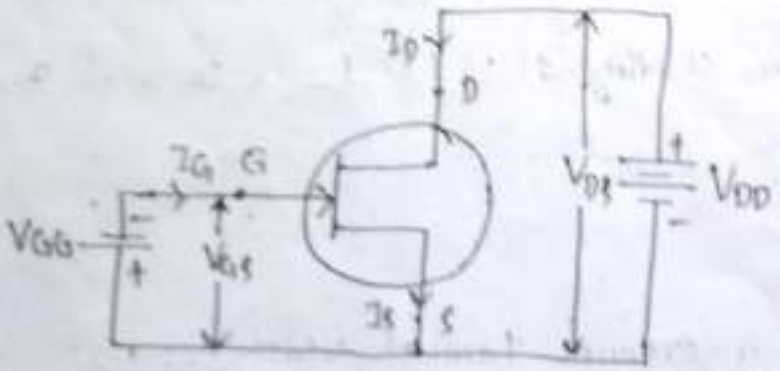
(i) For formation of N-channel JFET, a narrow bar of n-type semiconductor material is taken.

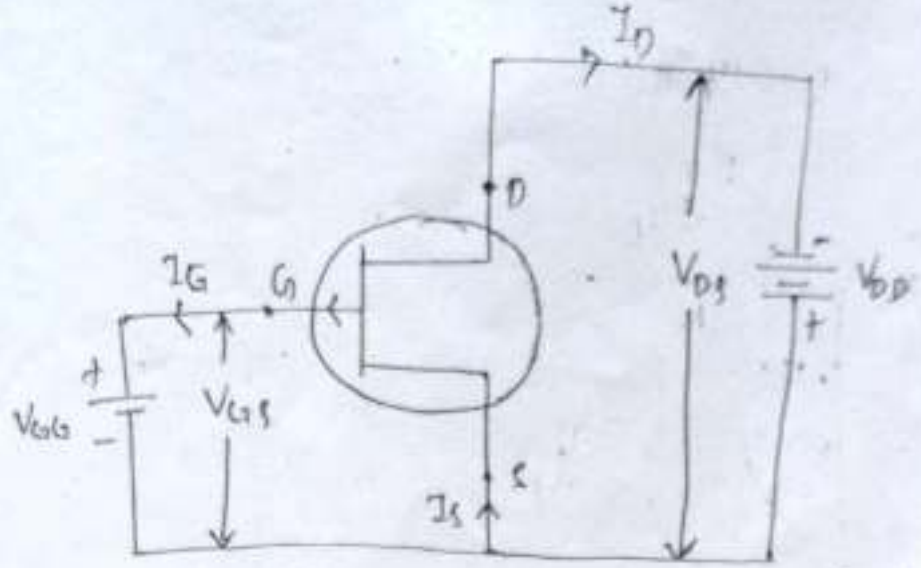
(ii) On the opposite sides of bar two heavily doped p-type semiconductor material is diffused to create two p-n junctions.

(iii) These heavily doped material are internally connected through a terminal called gate. The area between the gates is channel.

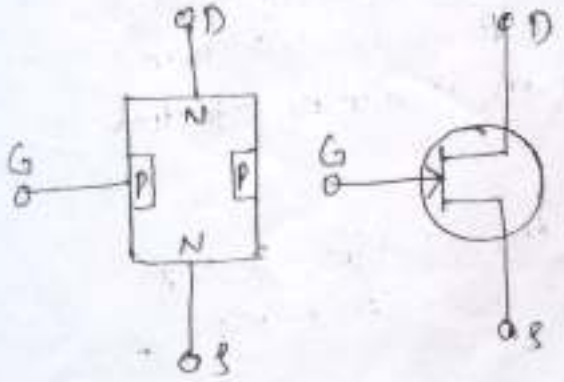
(iv) The other non-diffused terminal are called drain terminal & source terminal which may be interchanged.

CIRCUIT SYMBOL AND NOTATION:-

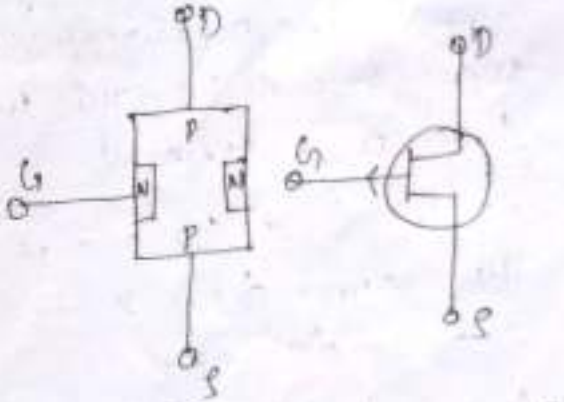




Here, V_{DD} is drain supply voltage
V_{DS} is drain to source voltage
V_{GG} is Gate supply voltage
V_{GS} is Gate to source voltage
I_D is drain current
I_S is source current
I_G is gate current

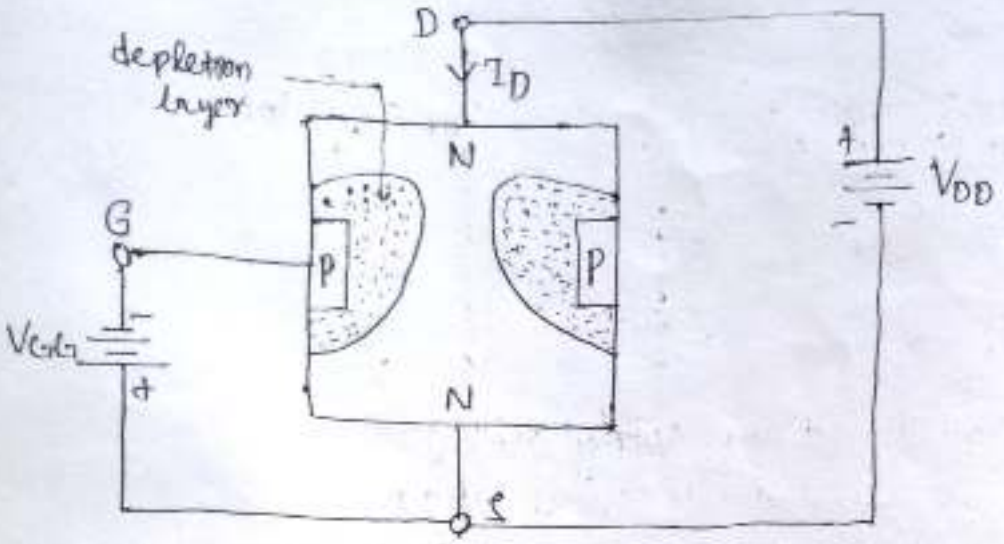


[N-CHANNEL JFET]



[P-CHANNEL JFET]

OPERATION OF N-CHANNEL JFET:→



(i) When 'V_{DD}' is applied without giving the gate to source voltage 'V_{GS}' a constant current which is maximum flows through the channel from drain to source.

(ii) When reverse 'V_{GS}' voltage is applied, the width of the depletion layer increases more at drain side than source side as the drain terminal is higher potential than source terminal.

(iii) At that time, the amount of current flows through the channel decreases because the width of the channel decreases.

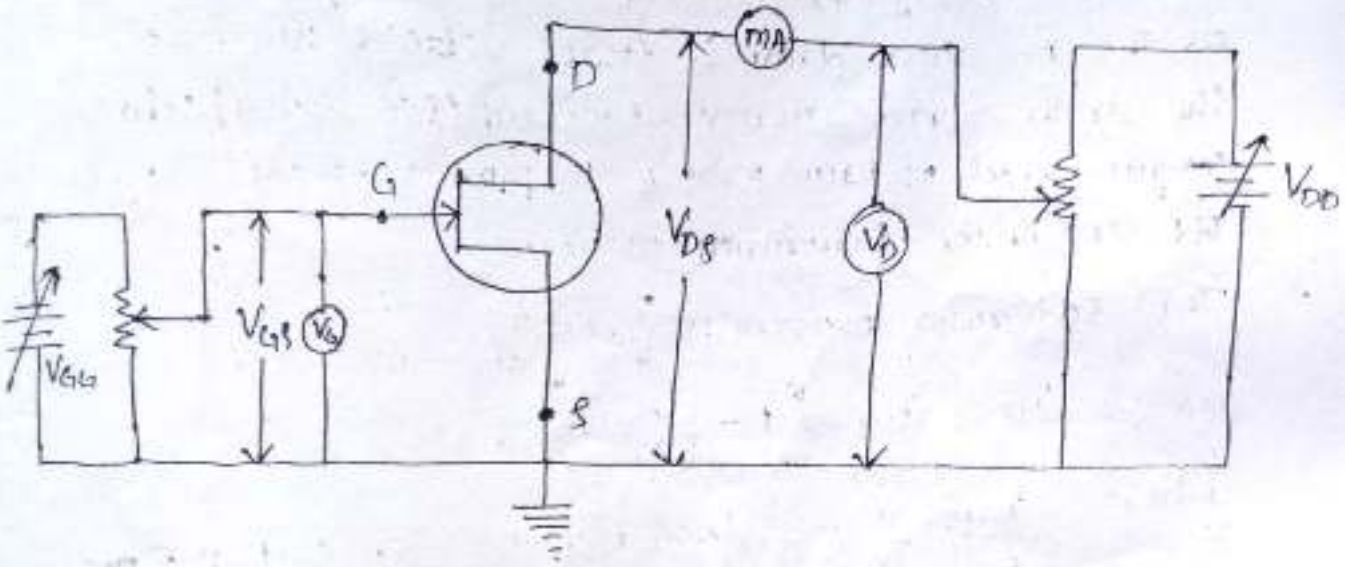
(iv) For a particular reverse voltage applied at gate to source terminal the depletion layer on both side will touch each other by reducing the width of the channel at that time, a pinch off path is formed through which a constant drain current flows from drain to source.

CHARACTERISTIC OF JFET :→

There are two types of characteristic in JFET i.e.

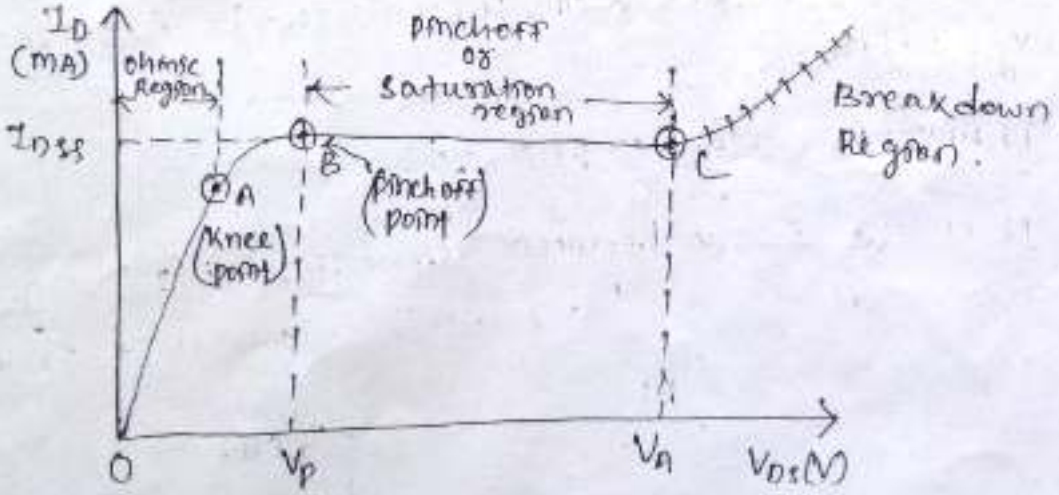
(a) Drain characteristic

(b). Transfer characteristic



DRAIN CHARACTERISTIC :—

It is the curve between drain current (I_D) & drain to source voltage 'V_{DS}' for different value of gate to source voltage 'V_{GS}'.



(i) Fig shows the drain characteristics of a JFET.

(ii) When V_{GS} is zero the I_D current increases linearly with the increase in 'V_{DS}' which shows a linear graph that is called Ohmic region up to the point 'A'.

(ii) As the voltage V_{DS} is progressively increased the drain current (I_D) increases at reverse square law rate up to the point 'B'. This point is called pinch off point.

(iii) The voltage at which the pinch off point occurs is called pinch off voltage (V_p). Thus pinch off voltage is defined as the minimum drain to source voltage at which the drain current remain constant (saturation). This region which is from point 'B' to point 'C' is called pinch off region or, saturation region.

The saturation current is given by

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$

where, I_{DSS} is the drain current when gate is shorted to source.

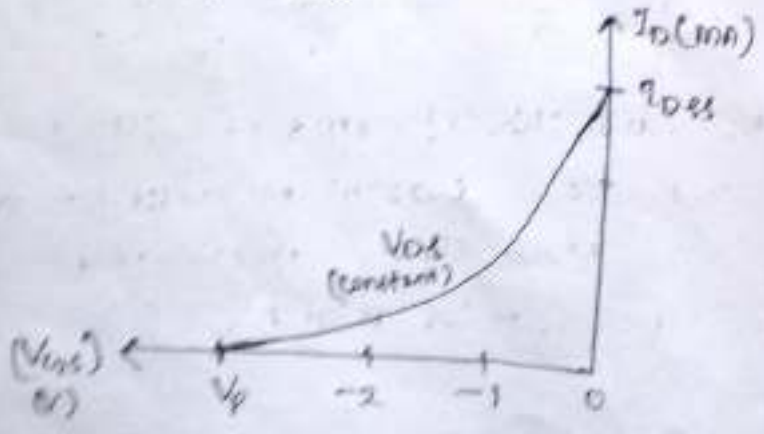
V_{GS} is voltage between gate & source

V_p is pinch off voltage.

(iv) With continued increase of V_{DS} after point 'C' avalanche breakdown occurs & the current suddenly increases to high value.

TRANSFER CHARACTERISTIC :→

It is the curve between drain current (I_D) & gate to source voltage (V_{GS}) for different values of drain to source voltage (V_{DS}).



(i) Fig shows the transfer characteristic of JFET.
(ii) Here, drain current is taken for different values of gate to source voltage at constant (V_{DS}).
(iii) When V_{GS} is zero, $I_D = I_{DSS}$ i.e. maximum current.
When $V_{GS} = V_P$ the I_D is zero.

FET PARAMETERS :→

DC DRAIN RESISTANCE :- (R_{DS})

It is the static or, ohmic resistance of the channel. It is the ratio of drain to source voltage to drain current.

i.e. $$R_{DS} = \frac{V_{DS}}{I_D}$$

AC DRAIN RESISTANCE :- (r_{ds})

It is the resistance between drain & source terminal when FET is operating in pinch off region which is given by

$$r_{ds} = \frac{\Delta V_{DS}}{\Delta I_D}$$

TRANSCONDUCTANCE :-

It is the ratio between change in drain current & change in gate to source voltage & is given by

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$$ at constant V_{DS}

It determines the slope of transfer characteristics of JFET.
The unit is siemens (S)

Expression for transconductance :→

We know that $$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Differentiate the I_D w.r.t V_{GS}

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$\Rightarrow \frac{d}{dV_{GS}}(I_D) = \frac{d}{dV_{GS}} I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$\Rightarrow \frac{\Delta I_D}{\Delta V_{GS}} = I_{DSS}\, 2\left[1-\frac{V_{GS}}{V_P}\right]\cdot\frac{d}{dV_{GS}}\left(1-\frac{V_{GS}}{V_P}\right)$$

$$= I_{DSS}\, 2\left(1-\frac{V_{GS}}{V_P}\right)\cdot\left(\frac{-1}{V_P}\right)$$

$$\therefore \frac{\Delta I_D}{\Delta V_{GS}} = \frac{-2 I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$$

g_{fs} or, $g_m = \frac{-2 I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$

When V_{GS} is zero

$$g_m = g_{m0} = \frac{-2 I_{DSS}}{V_P}$$

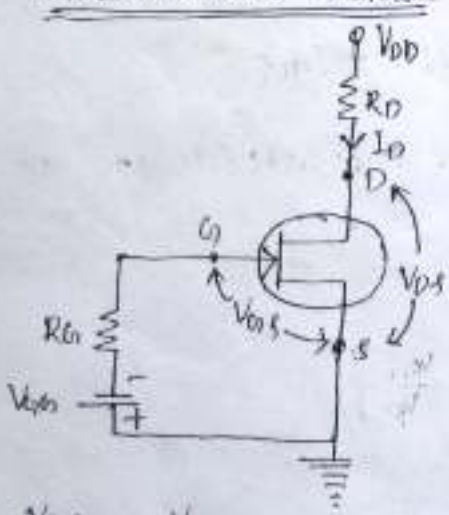
$$\Rightarrow g_m = g_{m0}\left(1-\frac{V_{GS}}{V_P}\right)$$

BIASING OF FET :-

There are different biasing technique such as

(a) Fixed biased method
(b) Self biased method
(c) Voltage divider biased method

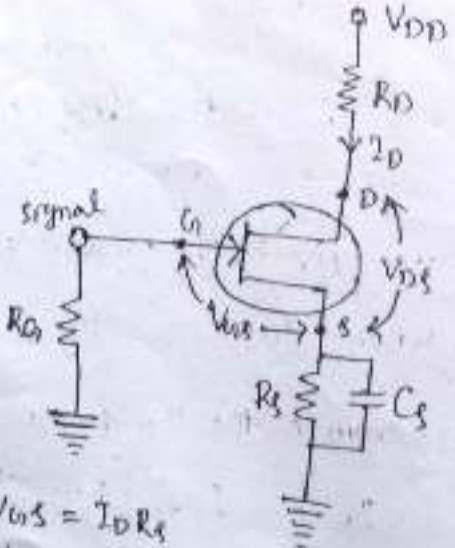
Fixed biased method



$V_{GS} = -V_{GG}$

$V_{DS} = V_{DD} - I_D R_D$

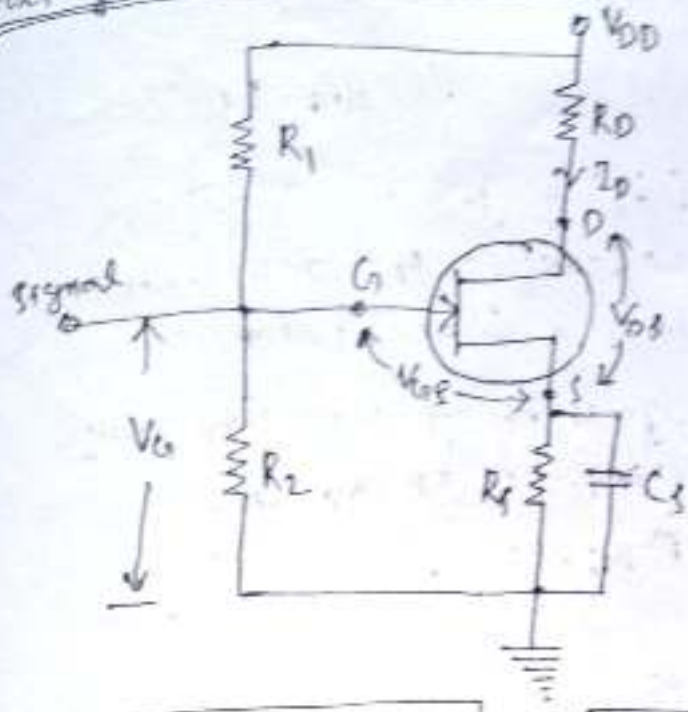
Self biased method



$V_{GS} = I_D R_S$

$V_{DS} = V_{DD} - I_D R_D - I_D R_S$.

voltage divider biased method:-



$$V_G = V_{DD} \times \frac{R_2}{R_1 + R_2}$$

$$I_D = \frac{V_{DD}}{R_D + R_S}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

(*) OPERATIONAL AMPLIFIERS :→

-|CHAPTER-05|-

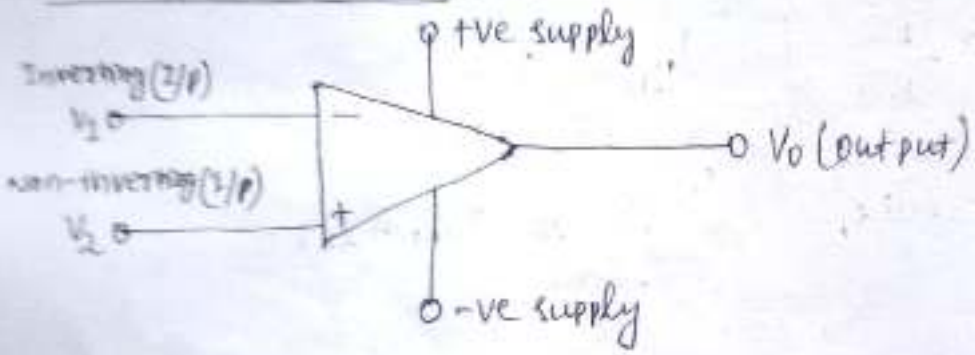
OP-AMP :-

(i) The OP-AMP is a direct coupled, high gain, -ve feedback amplifier which perform the mathematical operation such as addition, subtraction, integration & differentiation.

(ii) An OP-AMP can amplify the signals having frequency range from 0 Hz to 1 MHz. The examples of OP-AMP are

(a) IC 709, (b) LM 108, (c) IC 741 etc.

CKT SYMBOL OF OP-AMP :→



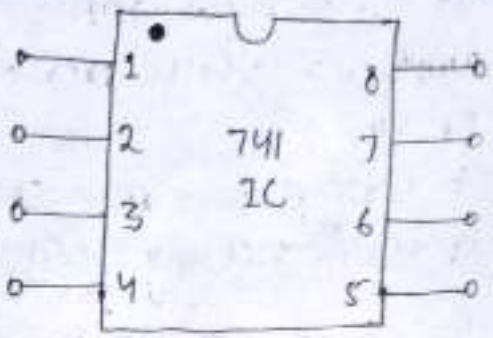
There are five terminals are present in an op-amp such as

(i) Inverting input terminal
(ii) Non-inverting input terminal
(iii) +ve supply terminal
(iv) -ve supply terminal
(v) output terminal.

When we given supply voltage at inverting input terminal then the OP-AMP can amplify the input voltage & gives output in the form of phase shift of input voltage.

When we given supply voltage at non-inverting input terminal then the OP-AMP can amplify the I/P voltage & gives O/P in the form of same phase of input voltage.

OP-AMP IC :- [PIN DIAGRAM]



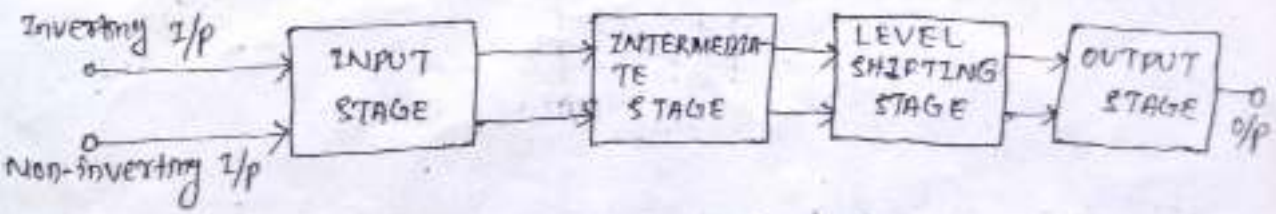
① → Offset null
② → Inverting input
③ → Non-inverting input
④ → -ve supply
⑤ → Offset null
⑥ → Output
⑦ → +ve supply
⑧ → Not Connected

CHARACTERISTIC OF IDEAL OP-AMP :→

(i) It has infinite voltage gain
(ii) It has infinite input resistance
(iii) It has zero output resistance
(iv) It has infinite bandwidth
(v) It gives the output voltage zero when equal voltages are applied at the input.
(vi) It has zero offset voltage

OPERATIONAL AMPLIFIER STAGES :→

BLOCK DIAGRAM OF OP-AMP :-



INPUT STAGE :→

(i) The input stage is a dual input, balanced output differential amplifier.
(ii) The function of differential amplifier is to provide high voltage gain to the op-amp.
(iii) It amplifies the difference between two input signals by rejecting all noise signals.

INTERMEDIATE STAGE :→

(i) It is a dual input, unbalanced output differential amplifier which provides some additional gain to the OP-Amp.

(ii) It acts as a direct coupling stage between input stage & level shifting stage.

LEVEL SHIFTING STAGE :–

(i) The level shifting stage is a emitter follower circuit which provides to maintain the DC level of amplifier.

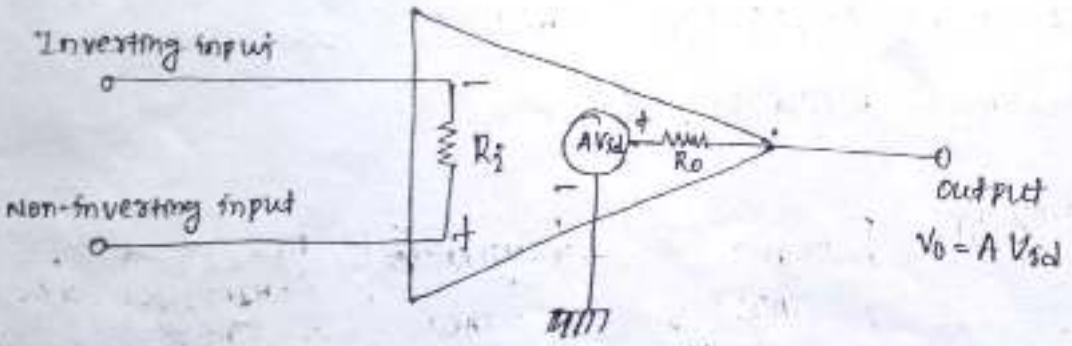
(ii) Its function is to shift the DC level to zero volt.

OUTPUT STAGE :–

(i) The output stage is generally a push-pull or, complimentary symmetry amplifier.

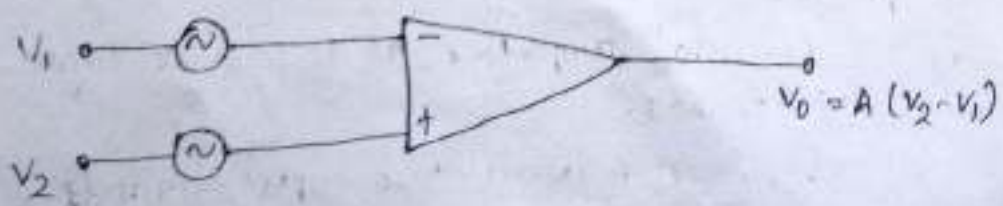
(ii) Its function is to increase large output swing of the amplifier with maintain of output resistance low.

EQUIVALENT CIRCUIT OF OP-AMP :→

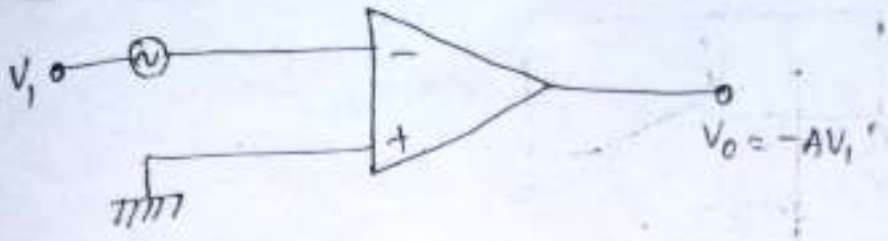


OPEN LOOP OP-AMP CONFIGURATION :→

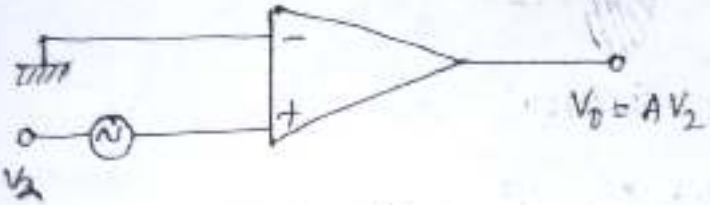
Differential OP-AMP :-



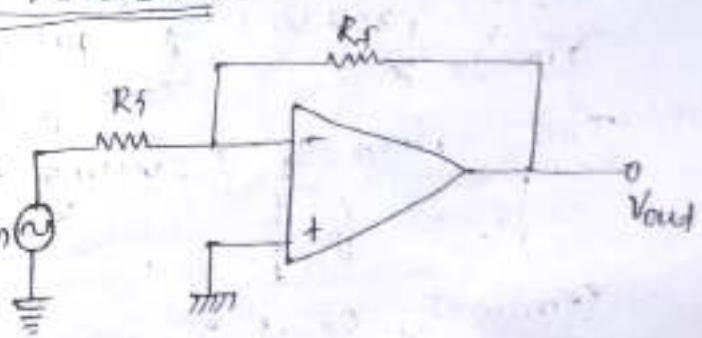
Inverting op-AMP :-



Non-inverting op-AMP :-



OP-AMP WITH NEGATIVE FEEDBACK :-

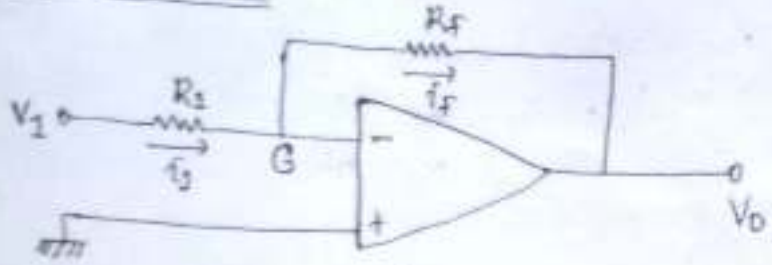


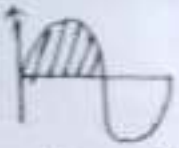
(i) An op-AMP is almost always operated with -ve feedback i.e. a part of the o/p is fed back in phase opposition to the input.

(*) The open-loop voltage gain of an op-AMP is very high (>100,000). Therefore, an extremely small input voltage drives the op-AMP into its saturated output stage.

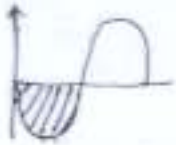
	VOLTAGE GAIN	INPUT Z	OUTPUT Z	BANDWIDTH
WITHOUT NEGATIVE FEEDBACK	A_{OL} is too high for linear amplifier applications	Relatively high	Relatively low	Relatively narrow
WITH NEGATIVE FEEDBACK	A_{CL} is set by the feedback ckt to desired value	can be increased or reduced to a desired value depending on type of ckt	can be reduced to a desired value	Significantly wider

INVERTING OP-AMP:-





[Input]



[OUTPUT]

(i) The voltage at point 'G' will become exactly zero when the -ve feedback voltage is exactly equal to the +ve voltage produced by input so this point is called virtual ground point. But actually it is not grounded.

(ii) The current i_1 is flowing through the point 'G' is given by

$$\boxed{i_1 = \frac{V_1}{R_1}}$$

Similarly, i_f is given by $\boxed{i_f = \frac{-V_o}{R_f}}$

At point 'G' $\frac{V_1}{R_1} = \frac{-V_o}{R_f}$

$$\Rightarrow \frac{-V_o}{V_1} = \frac{R_f}{R_1} \Rightarrow \boxed{\frac{V_o}{V_1} = \frac{-R_f}{R_1}}$$

(iii) This indicate the voltage gain of inverting amplifier

i.e. $\boxed{A_V = \frac{-R_f}{R_1}}$

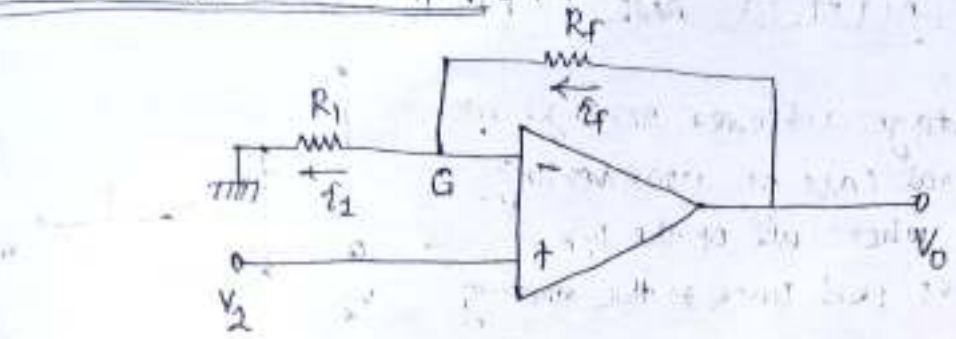
The following point may be noted about the inverting amplifier

(a) The closed-loop voltage gain is independent of the op-amp's internal open-loop voltage gain.

(b) If $R_1 = R_f$ then voltage gain of inverting amplifier can provide a unity voltage gain with 180° phase inversion.

(c) The inverting amplifier provides constant voltage gain.

NON-INVERTING OP-AMP:



(Input) (Output)

The current i_1 & i_f is given by

$$i_1 = \frac{V_2}{R_1} \qquad i_f = \frac{V_o - V_2}{R_f}$$

Applying KCL at point 'G'

$$i_f - i_1 = 0$$

$$\Rightarrow \frac{V_o - V_2}{R_f} - \frac{V_2}{R_1} = 0$$

$$\Rightarrow \frac{V_o - V_2}{R_f} = \frac{V_2}{R_1}$$

$$\Rightarrow \frac{V_o}{V_2} - 1 = \frac{R_f}{R_1}$$

$$\Rightarrow \boxed{\frac{V_o}{V_2} = 1 + \frac{R_f}{R_1}}$$

This indicate the voltage gain of non-inverting amplifier i.e.

$$\boxed{A_V = 1 + \frac{R_f}{R_1}}$$

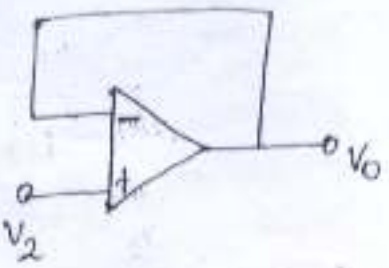
(a) The voltage gain of noninverting amplifier also depends upon the values of R_f & R_1.

(b) The voltage gain of a non-inverting amplifier can be made equal to or greater than 1.

(c) The voltage gain is positive. This is not surprising because output signal is in phase with the input signal.

VOLTAGE FOLLOWER AND BUFFER :→

(i) The voltage follower arrangement is a special case of noninverting amplifier where all of the o/p voltage is fed back to the inverting input.



(ii) In buffer amplifier the input voltage is equal to the output voltage with same phase.

(iii) It is required when a signal transferred from high impedance source to low impedance resistance with amplified form.

(iv) Here, the gain is unity & unity feedback is given from output to input. This ckt is also known as voltage follower or, source follower or, unit gain amplifier or, isolation amplifier.

OP-AMP PARAMETER :→

INPUT OFFSET VOLTAGE :→

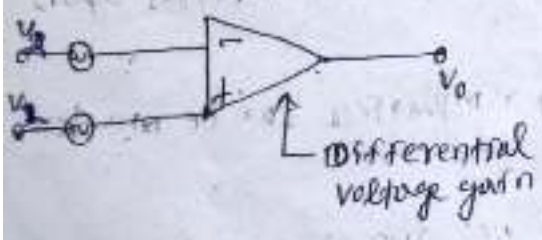
The input offset voltage is defined as the voltage that must be applied between the two terminals of OP-AMP to give zero output. Its range is from 1mv to 5mV.

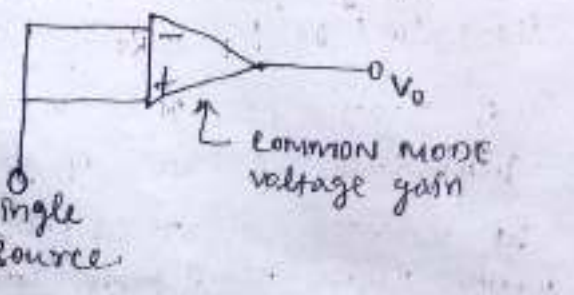
COMMON MODE REJECTION RATIO :→ [CMRR]

It is the ratio of differential voltage gain (A_d) to the common mode voltage gain (A_c) i.e.

$$CMRR = \frac{A_d}{A_c}$$

For ideal opamp, it must be '∞'.





SLEW RATE:-

It is defined as the max^m rate of change of output voltage per unit time i.e.

$$S.R = \frac{dV_o}{dt}$$

The unit of slew rate is volt per micro second

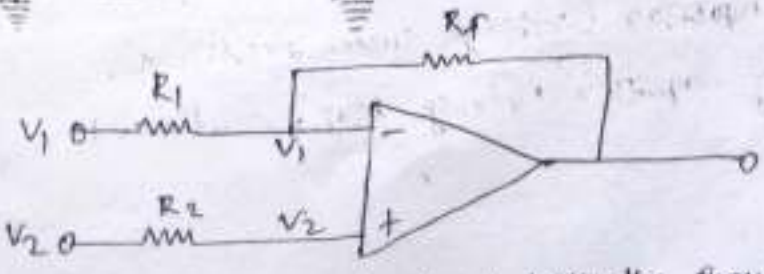
POWER SUPPLY/SUPPLY VOLTAGE REJECTION RATIO:- PSRR/SVRR

It is defined as the change in input offset voltage of OP-AMP caused by variation in supply voltage i.e.

$$PSRR = \frac{dV_{io}}{dV}$$

DIFFERENTIAL AMPLIFIER:-

The amplifier which accepts two input signals & amplifies the difference between these two signals is known as differential amplifier. (DA)



(i) Voltages are applied at both the input terminals of op-amp & their amplified difference appear at the o/p terminal.

(ii) Such a ckt is required when neither of the input leads is grounded.

(iii) The advantage of such an amplifier is that noise appearing at both the input terminals does not appear at the output.

⑧ OP-AMP WITH FEEDBACK :-

(i) The gain of open loop op-amp is very high so input signal of slightly greater than zero drives the output to saturation level.

(ii) Therefore, only the smaller signals, of the order our microvolts or, less having very low frequency can be amplified accurately without distortion.

(iii) The open loop gain of op-amp is not a constant. It varies high change in temperature & power supply

(iv) The op-Amp can be effectively utilized in linear applications by controlling the gain.

(v) This can be achieved by making use of feedback i.e. providing feedback from output to input either directly or via another network.

(vi) When the signal is feedback is in phase with the input signal, this is called positive feedback. Otherwise it is negative feedback.

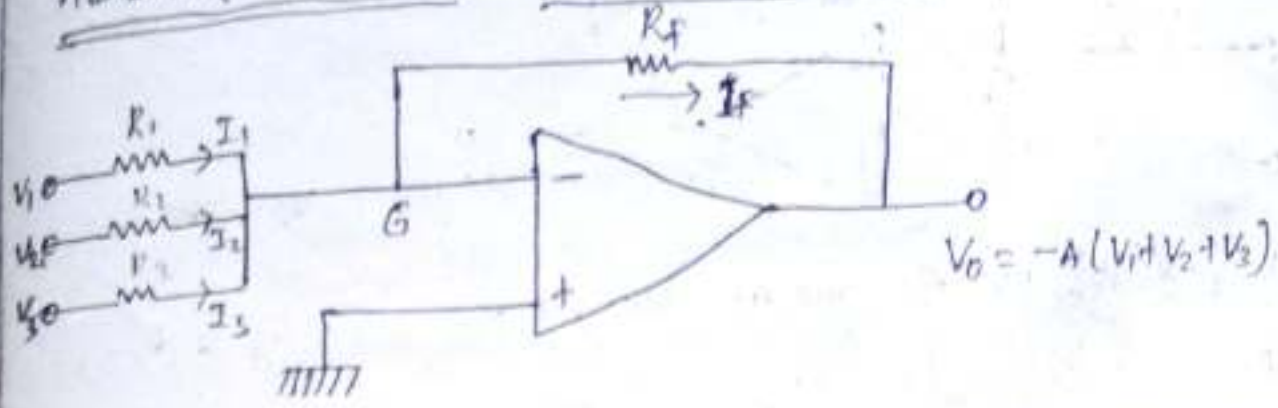
(vii) An op-amp that uses feedback is known as closed loop amplifier.

(viii) The most commonly used closed loop configuration are

(a) Inverting amplifier (voltage shunt feedback)

(b) Non-inverting amplifier (voltage series feedback).

ADDER OR SUMMING AMPLIFIER :→



As the point 'G' is virtually grounded the input currents are given by $I_1 = \frac{V_1}{R_1}$

$$I_2 = \frac{V_2}{R_2}$$

$$I_3 = \frac{V_3}{R_3}$$

The feedback current 'I_f' is given by $I_f = \frac{-V_0}{R_f}$

Applying KCL at point 'G', we get

$$I_1 + I_2 + I_3 = I_f$$

$$\Rightarrow \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} - \frac{-V_0}{R_f} = 0$$

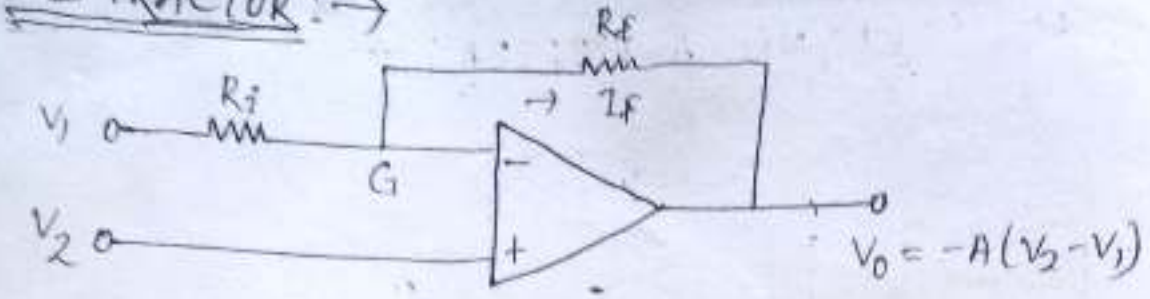
$$\Rightarrow \frac{V_0}{R_f} = \frac{-V_1}{R_1} - \frac{V_2}{R_2} - \frac{V_3}{R_3}$$

$$\Rightarrow V_0 = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$$

If $R_1 = R_2 = R_3 = R_f$

Then $\boxed{V_0 = -(V_1+V_2+V_3)}$

SUBTRACTOR :→



Let $(V_o)_1$ & $(V_o)_2$ are the output voltages produced by induced voltages V_1 & V_2 respectively.

Then $(V_o)_1 = \left(\frac{-R_f}{R_1}\right) V_1$

$(V_o)_2 = \left(1 + \frac{R_f}{R_1}\right) V_2$

$= \frac{R_f}{R_1}$ $\left[\because R_f >>> R_1\right]$

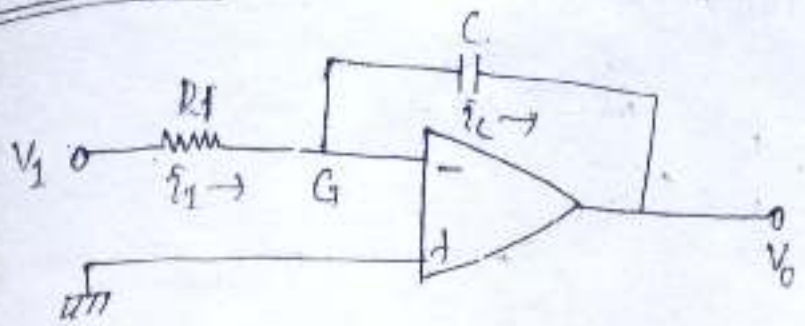
Then the output voltage is given by

$V_o = (V_o)_1 + (V_o)_2$

$V_o = \left(\frac{-R_f}{R_1}\right) V_1 + \frac{R_f}{R_1} V_2$

$$\boxed{V_o = \frac{R_f}{R_1}(V_2 - V_1)}$$

INTEGRATOR :-



The capacitive reactance is given by

$$x_c = \frac{1}{2\pi fC} = \frac{1}{j\omega C} = \frac{1}{sC}$$ where, $s = j\omega$ (in laplace notation)

From the fig, we conclude that

$$i_1 = \frac{V_1}{R_1}$$

$$i_c = \frac{-V_o}{x_c} = \frac{-V_o}{\frac{1}{sC}} = -V_o sC$$

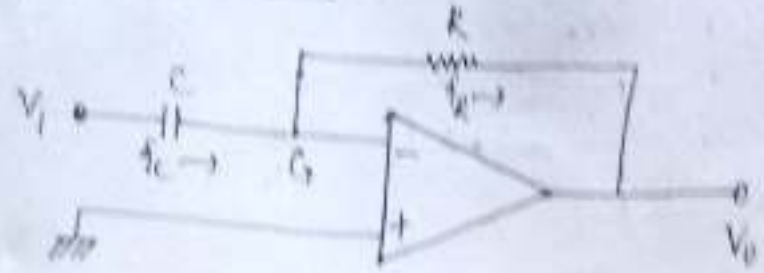
At point 'G', $i_1 = i_c$

$$\Rightarrow \frac{V_1}{R_1} = -V_o sC$$

$$\Rightarrow V_o = \frac{-V_1}{R_1 sC}$$

$$\Rightarrow \boxed{V_o(t) = \frac{-1}{R_1 C} \int V_1(t)\, dt}$$

DIFFERENTIATOR :→



The function of differentiator is to give an o/p voltage which is proportional to the rate of change of input voltage.

∴ we know that,

$$V_i = \frac{q}{C} \quad \text{where } q = \text{charge of capacitor}$$

$$\Rightarrow \frac{dV_i}{dt} = \frac{1}{C}\frac{dq}{dt}$$

$$\Rightarrow \frac{dV_i}{dt} = \frac{i}{C}$$

$$\Rightarrow i = C\frac{dV_i}{dt} \quad \text{--- (1) } \left[\text{where } i = \frac{dq}{dt}\right]$$

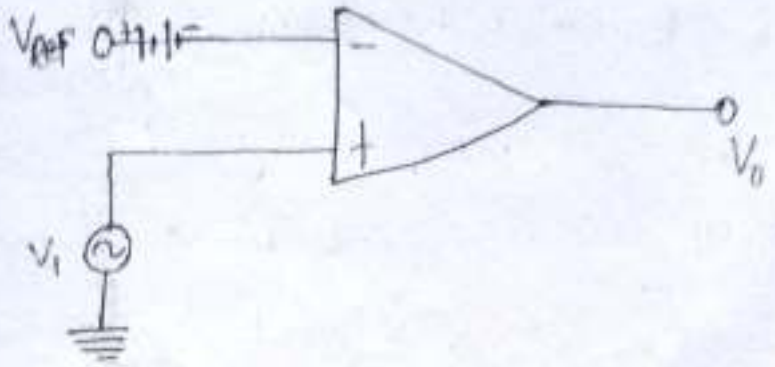
Again,

$$V_0 = -iR \quad \text{--- (2)}$$

putting eqn (1) in eqn (2), we get

$$\boxed{V_0 = -CR\frac{dV_i}{dt}}$$

COMPARATOR :→



→ Comparator is a ckt which compares two voltages & provides the output that indicates the relationship between them.

⇒ Comparators may be used to compare

(i) Two changing voltages like two sine waves

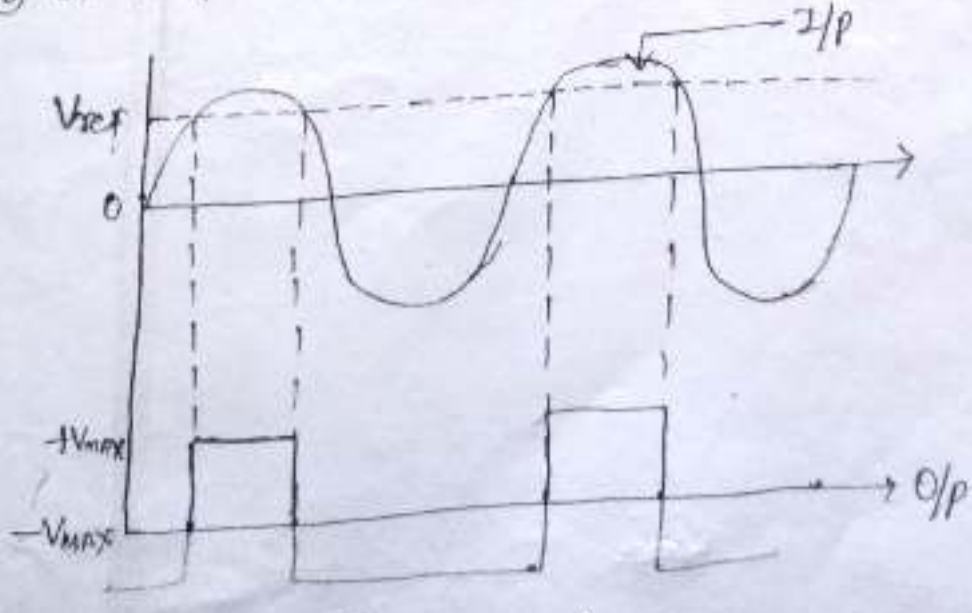
(ii) A changing voltage with a set D.C reference voltage.

⇒ The ckt for a compare along with its input & output waves forms is below.

⇒ A Comparator ckt has the following two characteristics

(a) It uses no feedback so that the voltage gain is equal to the open-loop voltage gain of Op-Amp.

(b) It is operated in a non-linear mode.



[WAVE FORMS]

⇒ The input voltage is applied to the non-inverting input terminal & ref d.c. reference voltage V_{ref} is applied to the inverting terminal of the op-amp. ...

⇒ As the open loop gain of op-Amp is very high.

⇒ Thus, the two possible output levels of this comparator are $+V_{sat}$ $(+V_{max})$ & $-V_{sat}$ $(-V_{max})$

⇒ The transition of V_o from $+V_{max}$ to $-V_{max}$ or vice-versa takes place when the input voltage V_i crosses the V_{ref} level.

= 0 =