

**UTKALMANI GOPABANDHU INSTITUTE OF**  
**ENGINEERING, ROURKELA**



LESSON PLAN

**SESSION: 2023-2024**

**DEPARTMENT OF ELECTRONICS AND**  
**TELECOMMUNICATION ENGINEERING**

**SUBJECT CODE: - Th.3**

**NAME OF THE SUBJECT: - MICROPROCESSOR & MICROCONTROLLER**

**BRANCH: - ELECTRONICS & TELECOMMUNICATIONS**

**SEMESTER: - DIPLOMA 4<sup>TH</sup> SEM**

**NUMBER OF CLASSES ALLOTTED PER WEEK: - 5**

**TOTAL PERIODS ALLOTTED TO THE SUBJECT ACCORDING TO AICTE: - 75**

**NAME OF THE FACULTY: - PRASANTA KUMAR DAKHINRAY**

# UTKALMANI GOPABANDHU INSTITUTE OF ENGINEERING, ROURKELA



## LESSON PLAN DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGINEERING

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**BRANCH: -** **ELECTRONICS & TELECOMMUNICATION**

**SEMESTER:** **DIPLOMA 4<sup>th</sup> SEM**

**PERIODS PER WEEK:-** 5

**NAME OF THE FACULTY: -** **PRASANTA KUMAR DAKHINRAY**  
**NO OF CLASSES ALLOTTED PER WEEK: -** 5 (16/01/2023 to 26/04/2024)

NO OF WEEKS	Lecture	Topic to be covered
1 <sup>st</sup> week	1 <sup>st</sup>	INTRODUCTION TO MICROPROCESSOR & MICROCOMPUTER & DIFFERENCE BETWEEN THEM .
	2 <sup>nd</sup>	CONCEPT OF ADDRESS BUS ,DATA BUS ,CONTROL BUS & SYSTEM BUS
	3 <sup>rd</sup>	GENERAL BUS STRUCTURE BLOCK DIAGRAM OF INTEL 8085
	4 <sup>th</sup>	BASIC ARCHITECTURE OF INTEL 8085 (8 BIT) MICROPROCESSOR.
	5 <sup>TH</sup>	Describe pin configuration of INTEL 8085.
2 <sup>nd</sup> week	1 <sup>st</sup>	DESCRIBE PIN DIAGRAM OF INTEL 8085 MICROPROCESSOR.
	2 <sup>nd</sup>	DISCUSS REGISTER ORGANISATION OF INTEL 8085 MICROPROCESSOR.
	3 <sup>rd</sup>	DISCUSS DIFFERENCE BETWEEN SPR & GPR.

	4 <sup>th</sup>	TIMING & CONTROL MODULE OF INTEL 8085 MICROPROCESSOR.
	5 <sup>th</sup>	WHAT STACK, STACK POINTER & STACK TOP.
3 <sup>rd</sup> week	1 <sup>st</sup>	DISCUSS 8085 INTERRUPTS.
	2 <sup>nd</sup>	DISCUSS MASKING OF INTERRUPTS (SIM, RIM)
	3 <sup>rd</sup>	DOUET CHACTER -1
	4 <sup>th</sup>	UNIT: - 2 INTRODUCTION SET & ASSRMBLY LANGUAGE PROGRAMMING .
	5 <sup>th</sup>	DISCUSS ADDRESSING DATA & ONE-BYTE, TWO-BYTE, &THREE-BYTE INSTRUCTION.



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**PERIODS PER WEEK: 5**

**NAME OF THE FACULTY PRASANTA KUMAR DAKHINRAY**

**NO OF CLASSES ALLOTTED PER WEEK: 5 (16/01/2024 to 26/04/2024)**

4 <sup>th</sup> week	1 <sup>st</sup>	DISCUSS ADDRESSING MODES IN INSTRUCTION WITH EXAMPLES.
	2 <sup>nd</sup>	INSTRUCTION SET OF 8085 (DATA TRANSFER, ARITHMETIC, LOGICAL)
	3 <sup>rd</sup>	BRANCHING, STACK & I/O, MACHINE CONTROL)
	4 <sup>th</sup>	SIMPLE ASSEMBLY LANGUAGE PROGRAMMING OF 8085 a) SIMPLE ADDITION & SUBTRACTION .
	5 <sup>th</sup>	LOGICAL OPERATIONS (AND, OR, COMPLEMENT 1S & 2S.& MASKING OF BITS.
5 <sup>th</sup> week	1 <sup>st</sup>	COUNTERS & TIME DELAY (SINGLE REGISTER, REGISTER PAIR & MORE THAN TWO REGISTER)
	2 <sup>nd</sup>	LOOPING, COUNTING & INDEXING (CALL /JMP ETC)
	3 <sup>rd</sup>	WHAT IS STACK & SUBROUTINE PROGRAMS.& CODE CONVERSION , BCD ARITHMETIC & 16 BIT DATA OPERATION , BLOCK TRANSFER .

	4 <sup>th</sup>	COMPARE BETWEEN TWO NUMBERS.
	5 <sup>th</sup>	ARRAY HANDLING (LARGEST NUMBER & SMALL
6 <sup>th</sup> week	1 <sup>st</sup>	DRAM TIMING DIAGRAM FOR MEMORY READ, MEMORYWRITE, I/O READ & I/O WRITE MACHINE CYCLE.
	2 <sup>nd</sup>	DRAW A NEAT SKETCH FOR THE TIMING DIAGRAM FOR INTEL 8085 INSTRUCTION (MOV, MVI, INSTRUCTION).
	3 <sup>rd</sup>	DRAW A NEAT SKETCH FOR THE TIMING DIAGRAM FOR INTEL 8085 INSTRUCTION LDA INSTRUCTION.
	4 <sup>th</sup>	DISCUSS MEMORY & I/O ADDRESSING
	5 <sup>th</sup>	<p style="text-align: center;"><b>UNIT: - 3</b></p> <p>DEFINE OPCODE ,OPERAND ,T-STATE ,FETCH CYCLE ,MACHINE CYCLE , INSTRUCTION CYCLE &amp; DISCUSS THE CONCEPT OF TIMING DIAGRAMS .</p>

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**NAME OF THE FACULTY: - PRASANTA KUMAR DAKHINRAY**

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<b>Week/Date</b>	<b>Lecture</b>	<b>Topic to be covered</b>
7 <sup>th</sup> week	1 <sup>st</sup>	<b>UNIT -4</b> CONCEPT OF INTERFACING ,DIFINE MAPPING & DATA TRANSFER MECHANISMS :-MEMORY MAPPING & I/O MAPPING .
	2 <sup>nd</sup>	CONCEPT OF MEMORY INTERFACING :- INTERFACING EPROM & RAM MEMORIES .
	3 <sup>rd</sup>	CONCEPT OF ADDRESS DECODING FOR I/O DEVICES. & PPI (INTEL 8255)
	4 <sup>th</sup>	GENERATE SQUARE WAVES ON ALL LINES OF INTEL 8255.
	5 <sup>th</sup>	ADC& DAC WITH INTERFACING .
8 <sup>th</sup> week	1 <sup>st</sup>	INTERFACING SEVEN SEGMENT DISPLAYS & GENERATE SQUARE WAVE ON ALL LINES OF INTEL 8255 .

	2 <sup>nd</sup>	DESIGN INTERFACE A TRAFFIC LIGHT CONTROL SYSTEM USING INTEL 8255 .
	3 <sup>rd</sup>	DESIGN INTERFACE FOR STEPPER MOTOR COTROL USING INTEL 8255.
	4 <sup>th</sup>	BASIC CONCEPT OF OTHER INTERFACING DMA CONTROLLER : (USART)
	5 <sup>th</sup>	<b>UNIT -5</b> MICROPROCESSOR (ARCHITECTURE & PROGRAMMING -8086 -16 BIT) REGISTER ORGANISATION OF INTEL 8086.
9 <sup>th</sup> week	1 <sup>st</sup>	INTERNAL ARCHITECTURE OF INTEL 8086.
	2 <sup>nd</sup>	DISCUSS SIGAL DESCRIPTION OF INTEL 8086.
	3 <sup>rd</sup>	GENERAL BUS OPERATION & PHYSICAL MEMORY ORGANISATION
	4 <sup>th</sup>	WHAT IS MINIMUM MODES & TIMINGS.
	5 <sup>th</sup>	WHAT IS MAXIMUM MODES & TIMINGS.



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10 <sup>TH</sup> week	1 <sup>st</sup>	DISCUSS INTERRUPTS & INTERRUPTS SERVICE ROUTINES.
	2 <sup>nd</sup>	WHAT IS INTERRUPT CYCLE & ALSO NON-MASKABLE INTERRUPT.
	3 <sup>rd</sup>	WHAT IS MASKABLE INTERRUPT. & ALSO INTEL 8086 INSTRUCTION SET.



	4 <sup>th</sup>	PROGRAMMING ADDRESSING MODES & INSTRUCTION SET.
	5 <sup>th</sup>	ASSEMBLRE DIRECTIVES & OPERATIONS.
11 <sup>th</sup> week	1 <sup>st</sup>	SIMPLE ASSEMBLY LANUGUAGE PROGRAMMING OF INTEL 8086 INSTRUCTION .
	2 <sup>nd</sup>	SIMPLE ASSEMBLY LANUGUAGE PROGRAMMING OF INTEL 8086 INSTRUCTION .
	3 <sup>rd</sup>	SIMPLE ASSEMBLY LANUGUAGE PROGRAMMING OF INTEL 8086 INSTRUCTION .
	4 <sup>th</sup>	<u>UNIT: - 6</u>
	5 <sup>th</sup>	INTRODUCTION TO MICRO CONTROLLER ( INTEL 5051) DISCUSS DIFFERENENT BETWEEN MICROPROCESSOR & MICROCONTROLLER & ALSO 8-BIT & 16-BIT MICROCONTROLLER.
12 <sup>th</sup> week	1 <sup>st</sup>	WHAT DO MEAN BY CISC &RISC PROCESSOR.
	2 <sup>nd</sup>	ARCHITECTURE OF INTEL 8051 MICROCONTROLLER .
	3 <sup>rd</sup>	AGAIN REPEAT ARCHITECTURE OF INTEL 8051 MICROCONTROLLER.
	4 <sup>th</sup>	DISCUSS SIGNAL DESCRIPTION OF INTEL 8051 MICROCONTROLLER .
	5 <sup>th</sup>	DISCUSS MEMORY ORGANISATION OF RAM STRUCTURE.
13 <sup>th</sup> week	1 <sup>st</sup>	DISCUSS MEMORY ORGANISATION OF SFR .
	2 <sup>nd</sup>	EXPLAIN REGISTERS OF INTEL8051 MICROCONTROLLER .
	3 <sup>rd</sup>	EXPLAIN TIMERS OF INTEL8051 MICROCONTROLLER
	4 <sup>th</sup>	DISCUSS INTERRUCTS OF INTEL 8051 MICROCONTROLLRE .
	5 <sup>th</sup>	DISCUSS VARIOUS ADDRESSING MODES OF INTEL 8051 MICROCONTROLLER .
14 <sup>th</sup> week	1 <sup>st</sup>	SIMPLE INTEL 8051 ASSEMBLY LANUAGE PROGRAMMING OF ARITHMETIC INSTRUCTION .
	2 <sup>nd</sup>	SIMPLE INTEL 8051 ASSEMBLY LANUAGE PROGRAMMING OF LOGIC INSTRUCTION
	3 <sup>rd</sup>	SIMPLE INTEL 8051 ASSEMBLY LANUAGE PROGRAMMING OF A JUMP INSTRUCTION.

	4 <sup>th</sup>	SIMPLE INTEL 8051 ASSEMBLY LANGUAGE PROGRAMMING OF A LOOP INSTRUCTION .
	5 <sup>th</sup>	SIMPLE INTEL 8051 ASSEMBLY LANGUAGE PROGRAMMING OF CALL INSTRUCTION
15 <sup>th</sup> Week	1 <sup>st</sup>	SIMPLE INTEL 8051 ASSEMBLY LANGUAGE PROGRAMMING OF I/O PORT PROGRAMMING
	2 <sup>nd</sup>	DISCUSS INTERRUPTS OF INTEL 8051 MICROCONTROLLER
	3 <sup>rd</sup>	. DISCUSS TIMER & COUNTERS OF INTEL 8051 MICROCONTROLLER & ALSO DISCUSS SEMSTER WISE QUESTIONS
	4 <sup>th</sup>	WRITE A PROGRAM TO ADDITION OF TWO, 8 BITS NUMBER & STORED THE RESULT IN THE MEMORY LOCATION
	5 <sup>th</sup>	. WRITE A PROGRAM TO SUBTRACTION OF TWO, 8 BITS NUMBER & STORED THE RESULT IN THE MEMORY LOCATION

16 <sup>th</sup> week	1 <sup>st</sup>	WRITE A PROGRAM TO SUBTRACTION OF TWO, 8 BITS NUMBER & STORED THE RESULT IN THE MEMORY LOCATION
	2 <sup>nd</sup>	WRITE A PROGRAM TO FIND 1S COMPLIMENTS OF 8 BIT NUMBER & RESULT WILL BE STORED IN THE MEMORY LOCATION.
	3 <sup>rd</sup>	WRITE A PROGRAM TO FIND 2S COMPLIMENTS OF 8 BIT NUMBER & RESULT WILL BE STORED IN THE MEMORY LOCATION
	4 <sup>th</sup>	WRITE A PROGRAM TO FIND LARGEST NUMBER IN DATA ARRAY & RESULT WILL BE STORED IN THE MEMORY LOCATION.
	5 <sup>th</sup>	WRITE A PROGRAM TO FIND SMALLEST NUMBER IN DATA ARRAY & RESULT WILL BE STORED IN THE MEMORY LOCATION.
17 <sup>th</sup> week	1 <sup>st</sup>	WRITE A PROGRAM TO SHIFT 8 BIT NUMBER LEFT BY 1 BITS & RESULT WILL BE STORED IN THE MEMORY LOCATION.

	2 <sup>nd</sup>	WRITE A PROGRAM TO SHIFT 8 BIT NUMBER LEFT BY 2 BITS & RESULT WILL BE STORED IN THE MEMORY LOCATION REVIEW UNIT- 1
	3 <sup>rd</sup>	REVIEW UNIT-2
	4 <sup>th</sup>	REVIEW UNIT-3
	5 <sup>th</sup>	REVIEW UNIT-4
18 <sup>th</sup> week	1 <sup>st</sup>	REVIEW UNIT-5
	2 <sup>nd</sup>	REVIEW UNIT-6
	3 <sup>rd</sup>	DISCUSS MCQ
	4 <sup>th</sup>	DISCUSS MCQ
	5 <sup>th</sup>	DISCUSS MCQ